

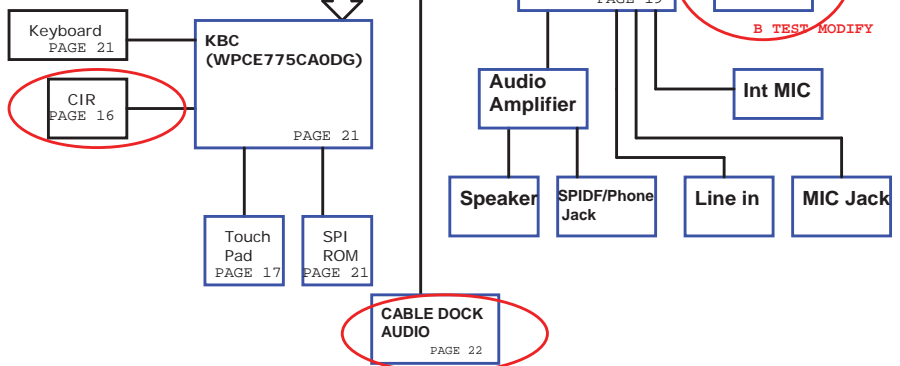
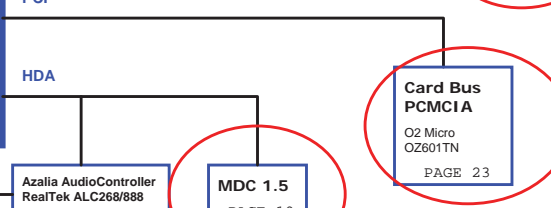
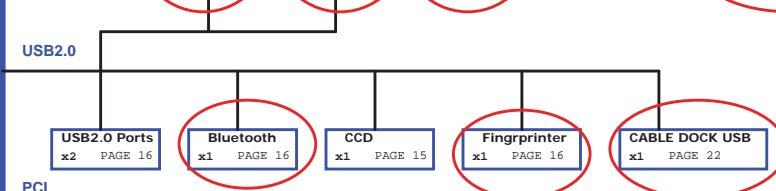
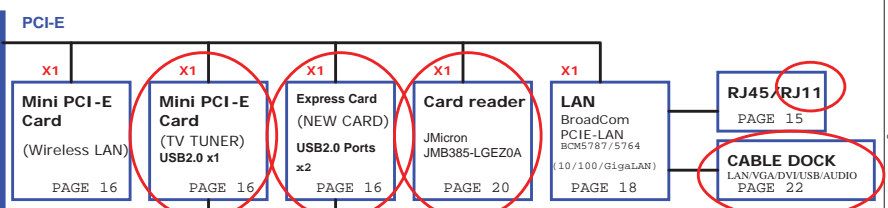
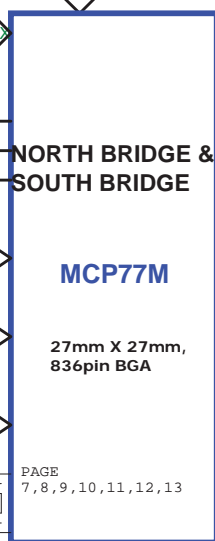
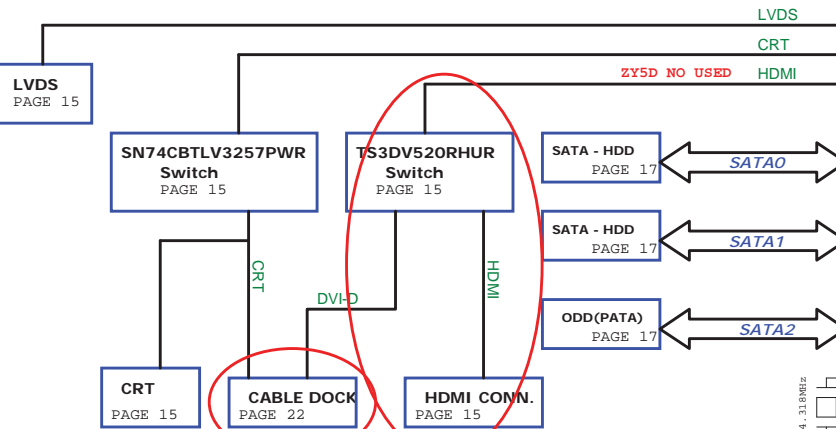
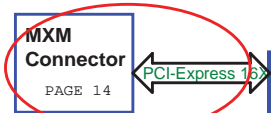
ZY5/ZY5D SYSTEM BLOCK DIAGRAM



- CPU CORE ISL6265A
PAGE 26
- NB CORE +1.1V
PAGE 27
- NB RUN +1.1V
PAGE 28
- DDR II SMD DR_VTERM
1.8VSUS(TPS51116REGR)
PAGE 29
- SYSTEM POWER
ISL6237
PAGE 25
- SYSTEM CHARGER
(ISL6251A)
PAGE 24
- DISCHARGER
/+1.1V_S5,+1.2V,+2.5V
PAGE 30



ZY5D NO USED



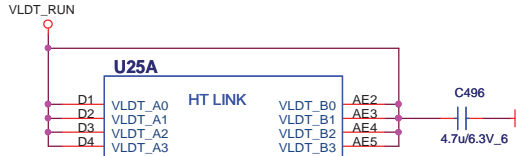
- PCB STACK UP
- LAYER 1 : TOP
 - LAYER 2 : SGND1
 - LAYER 3 : IN1
 - LAYER 4 : IN2
 - LAYER 5 : VCC
 - LAYER 6 : GND



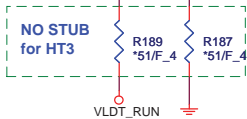
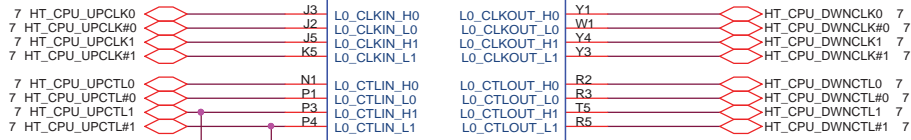
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

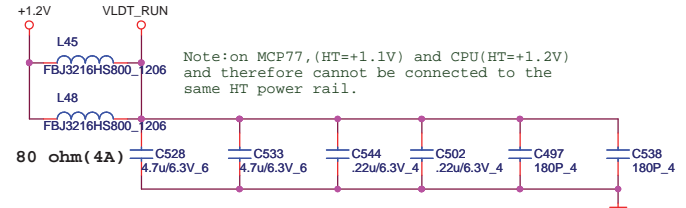
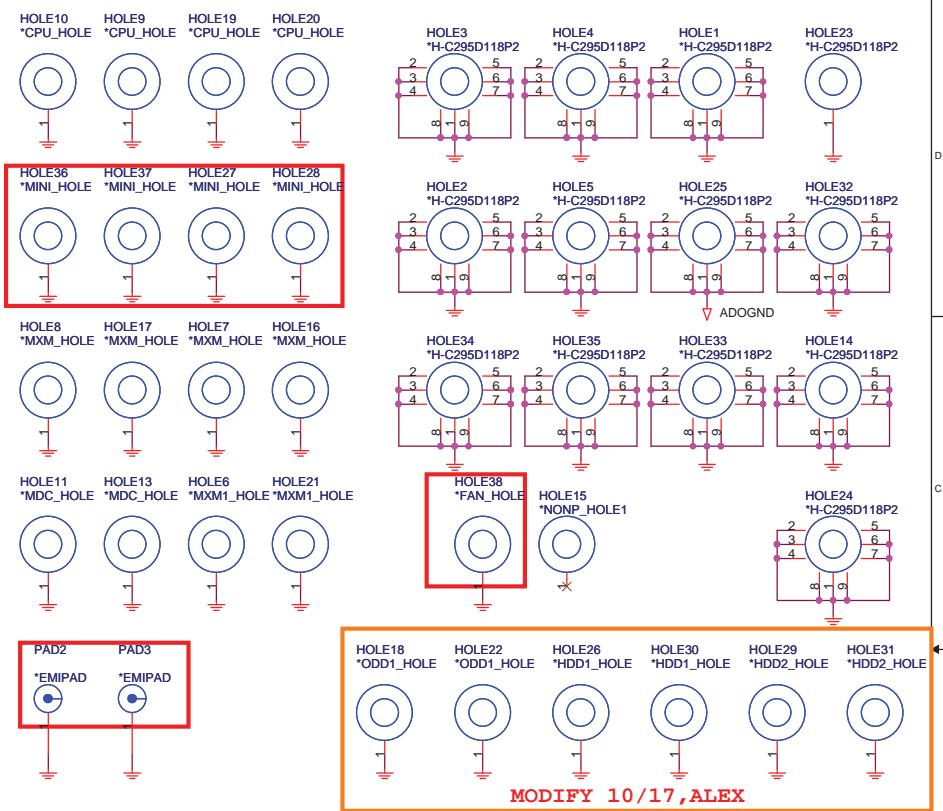
REV:B Modify



HT_RXD0	E3	L0_CADIN_H0	AD1	HT_TXD0
HT_RXD#0	E2	L0_CADIN_L0	AC1	HT_TXD#0
HT_RXD1	F1	L0_CADIN_H1	AC2	HT_TXD1
HT_RXD#1	F1	L0_CADIN_L1	AC3	HT_TXD#1
HT_RXD2	G3	L0_CADIN_H2	AB1	HT_TXD2
HT_RXD#2	G2	L0_CADIN_L2	AA1	HT_TXD#2
HT_RXD3	G1	L0_CADIN_H3	AA2	HT_TXD3
HT_RXD#3	H1	L0_CADIN_L3	AA3	HT_TXD#3
HT_RXD4	J1	L0_CADIN_H4	W2	HT_TXD4
HT_RXD#4	K1	L0_CADIN_L4	W3	HT_TXD#4
HT_RXD5	L3	L0_CADIN_H5	V1	HT_TXD5
HT_RXD#5	L2	L0_CADIN_L5	U1	HT_TXD#5
HT_RXD6	L1	L0_CADIN_H6	U2	HT_TXD6
HT_RXD#6	M1	L0_CADIN_L6	U3	HT_TXD#6
HT_RXD7	N3	L0_CADIN_H7	T1	HT_TXD7
HT_RXD#7	N2	L0_CADIN_L7	R1	HT_TXD#7
HT_RXD8	E5	L0_CADIN_H8	AD4	HT_TXD8
HT_RXD#8	F5	L0_CADIN_L8	AD3	HT_TXD#8
HT_RXD9	F3	L0_CADIN_H9	AD5	HT_TXD9
HT_RXD#9	F4	L0_CADIN_L9	ACS	HT_TXD#9
HT_RXD10	G5	L0_CADIN_H10	AB3	HT_TXD10
HT_RXD#10	H5	L0_CADIN_L10	AB4	HT_TXD#10
HT_RXD11	H3	L0_CADIN_H11	AB5	HT_TXD11
HT_RXD#11	H4	L0_CADIN_L11	AA5	HT_TXD#11
HT_RXD12	K3	L0_CADIN_H12	Y5	HT_TXD12
HT_RXD#12	K4	L0_CADIN_L12	W5	HT_TXD#12
HT_RXD13	L5	L0_CADIN_H13	V4	HT_TXD13
HT_RXD#13	M5	L0_CADIN_L13	V3	HT_TXD#13
HT_RXD14	M3	L0_CADIN_H14	V5	HT_TXD14
HT_RXD#14	M4	L0_CADIN_L14	U5	HT_TXD#14
HT_RXD15	N5	L0_CADIN_H15	T4	HT_TXD15
HT_RXD#15	P5	L0_CADIN_L15	T3	HT_TXD#15



Athlon 64 S1g2 SOCKET_638_PIN
 Athlon 64 S1g2
 Processor Socket
 SOCKET_638_PIN



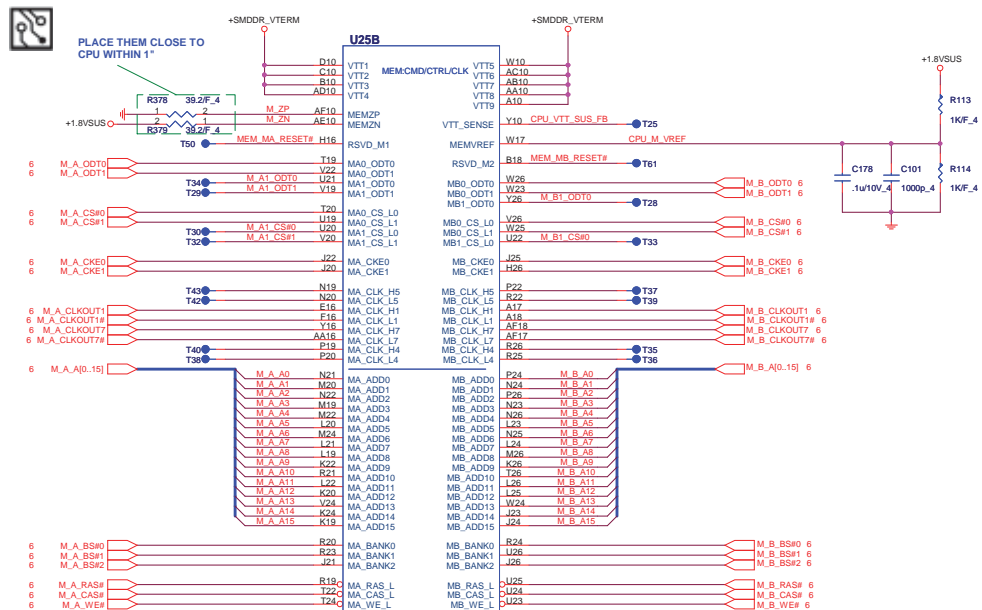
Note: on MCP77, (HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.

LAYOUT: Place bypass cap on topside of board
 NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
 PLACE CLOSE TO VLDT0 POWER PINS

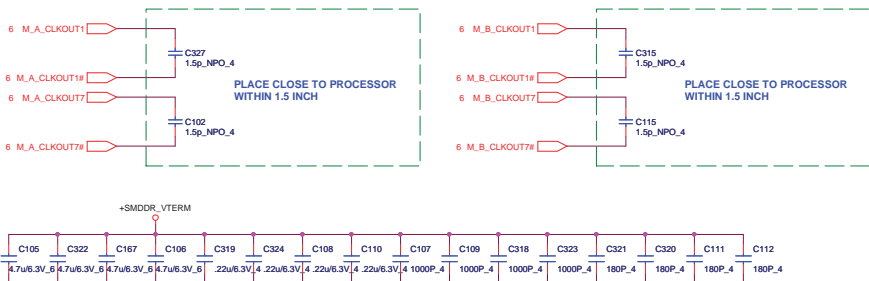
Quanta Computer Inc.
 PROJECT : ZY5D

Size	Document Number	AMD Griffin HT I/F	Rev
			3B
Date:	Wednesday, May 21, 2008	Sheet	2 of 35

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



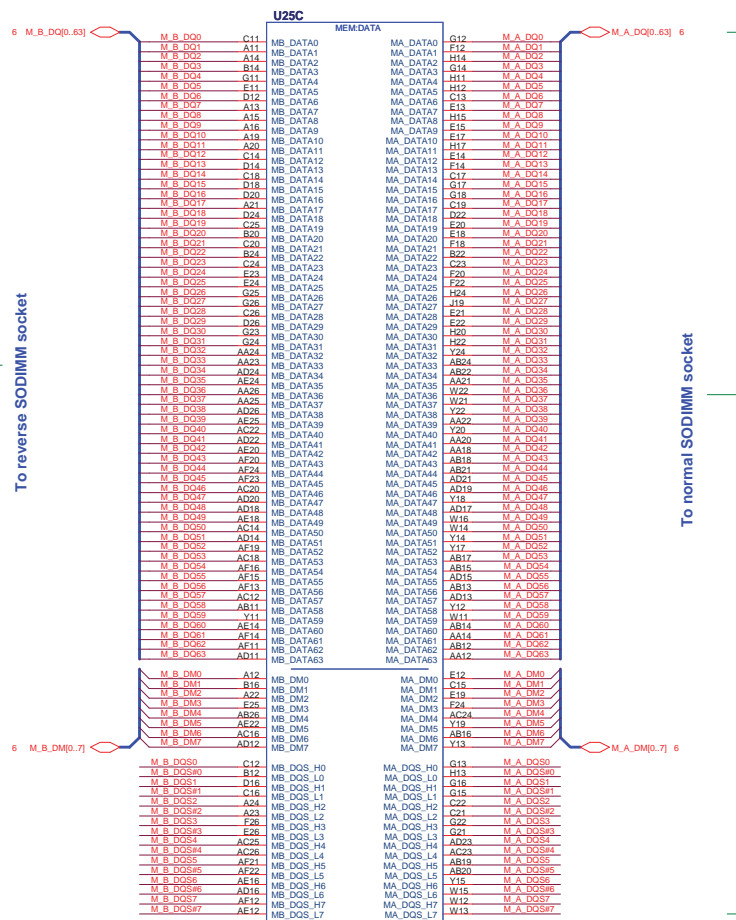
Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

Processor DDR2 Memory Interface



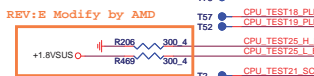
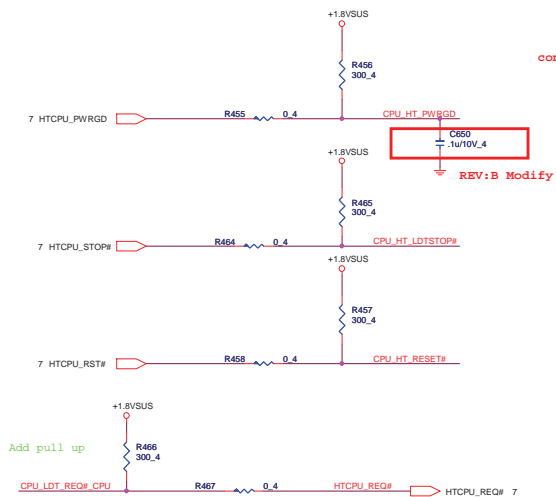
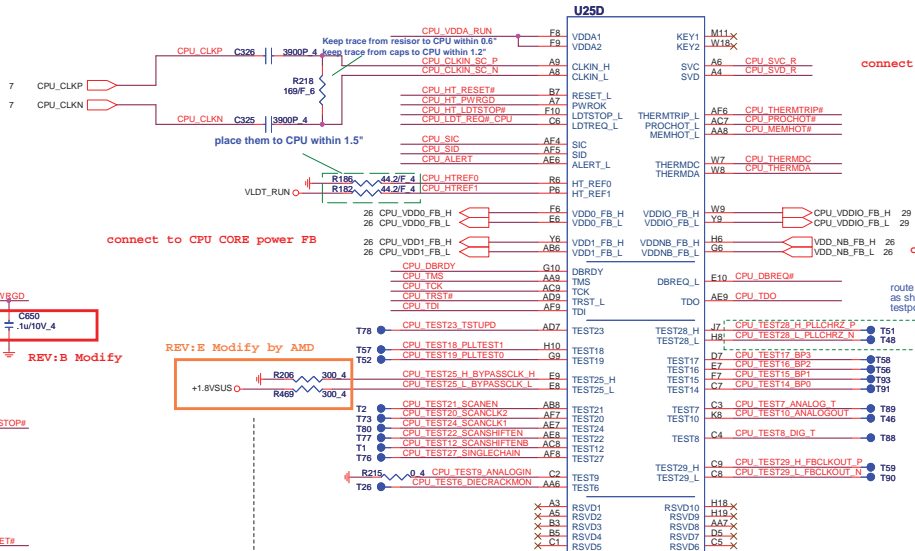
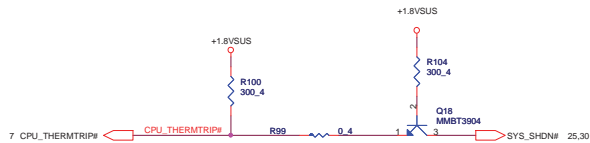
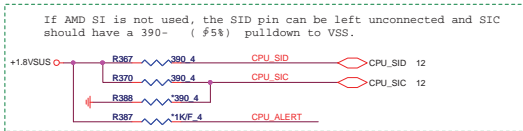
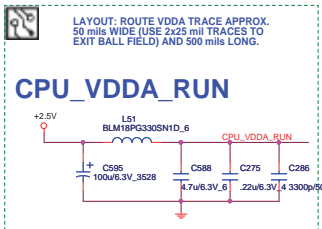
To reverse SODIMM socket

To normal SODIMM socket

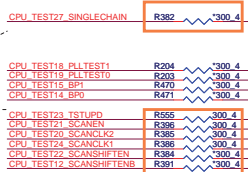
Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN



ATHLON Control and Debug



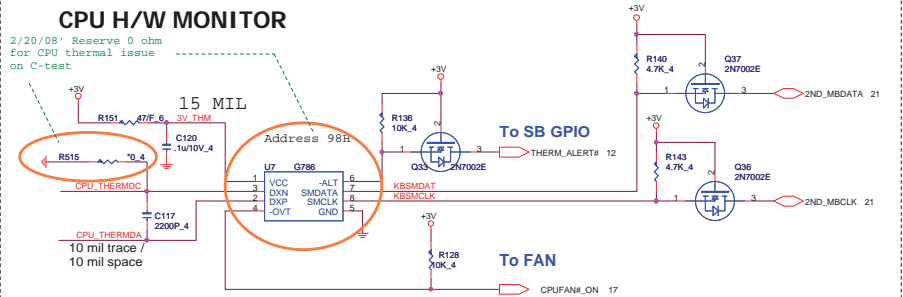
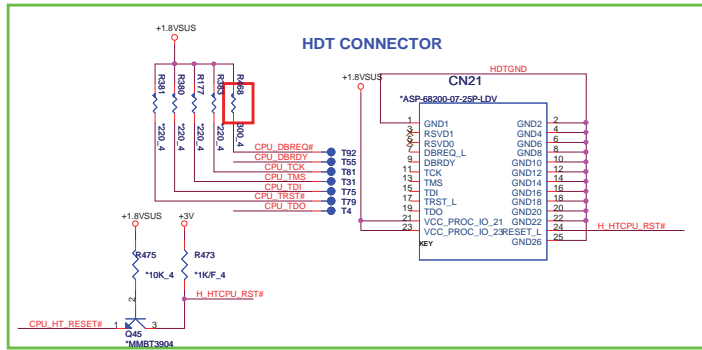
Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN



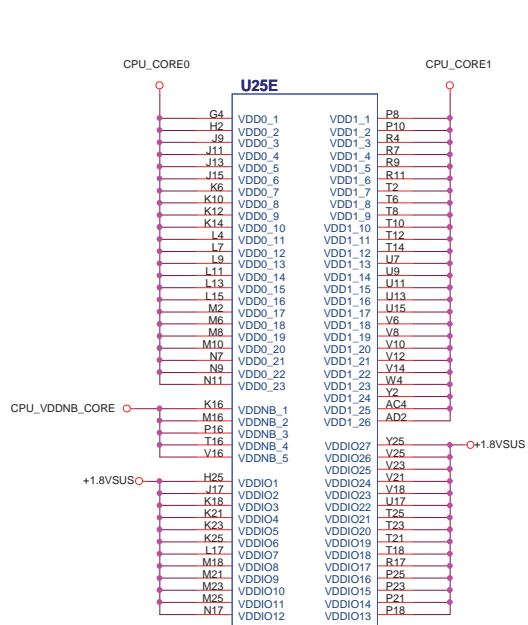
Rev:E Add R555 by AMD
Design guide 41650 V1_03
on 5/8.

VFIX MODE

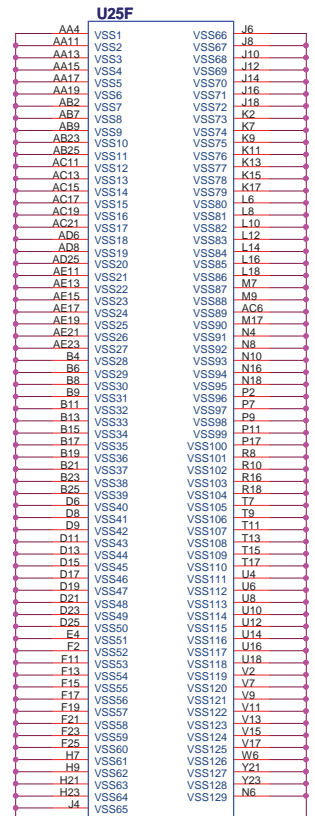
SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V



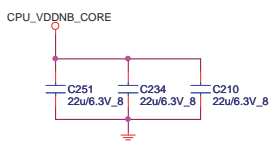
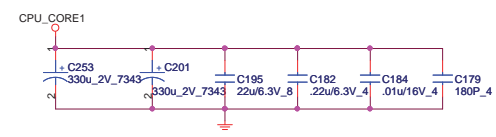
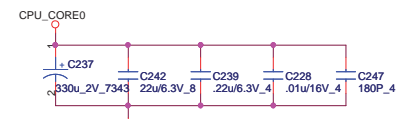
PROCESSOR POWER AND GROUND




Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN

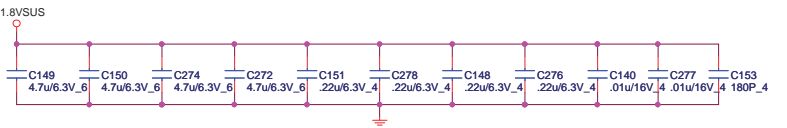


Athlon 64 S1g2 SOCKET_638_PIN
Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN





DECOUPLING BETWEEN PROCESSOR AND DIMMS PLACE CLOSE TO PROCESSOR AS POSSIBLE



+1.8VSUS

C148 4.7u/6.3V_6

C150 4.7u/6.3V_6

C274 4.7u/6.3V_6

C272 4.7u/6.3V_6

C151 22u/6.3V_4

C278 22u/6.3V_4

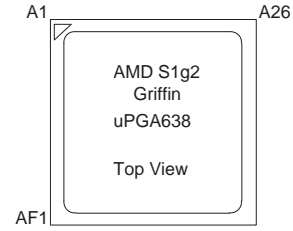
C148 22u/6.3V_4

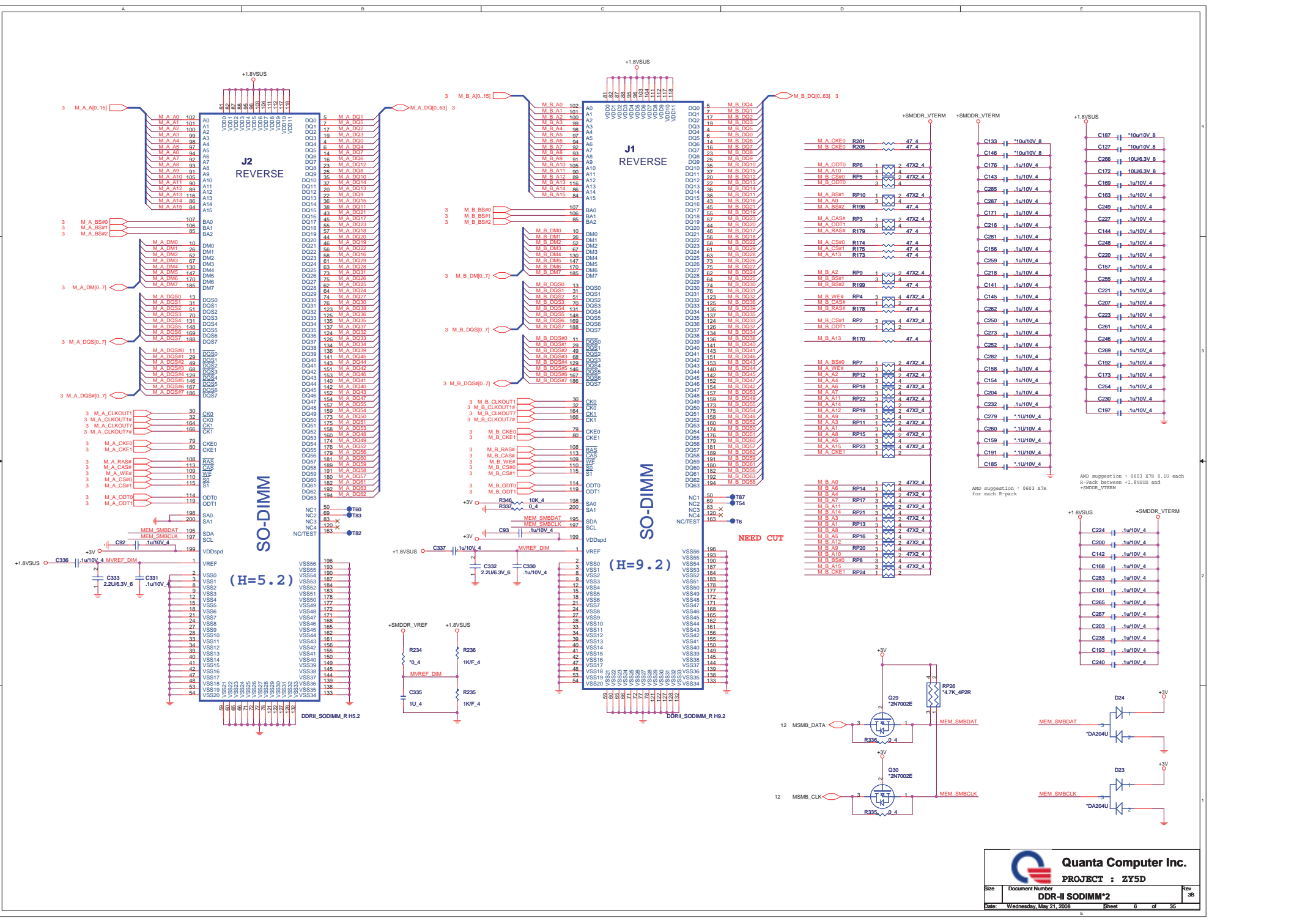
C276 22u/6.3V_4

C140 .01u/16V_4

C277 .01u/16V_4

C153 180P_4





AMD suggestion : 0603 XTR 0.1u each
R-Pack between +1.8VSS3 and
+SMDDR_VTERM

AMD suggestion : 0603 XTR
for each R-pack

Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	DDR-II SODIMM*2	38
Date	Wednesday, May 21, 2008	Sheet 6 of 35

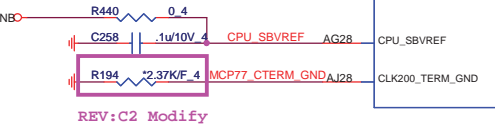
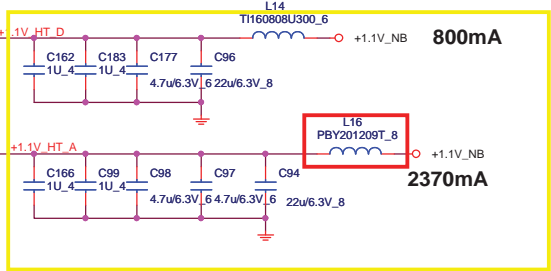
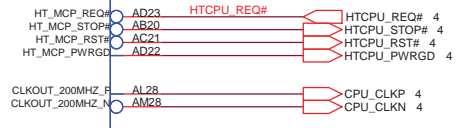
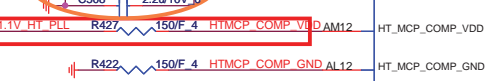
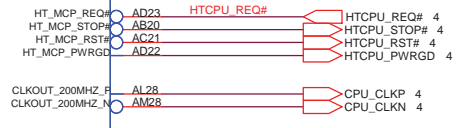
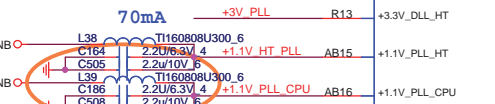
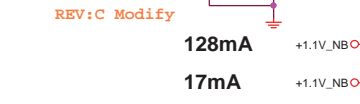
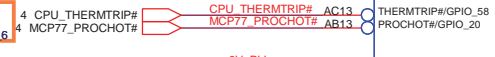
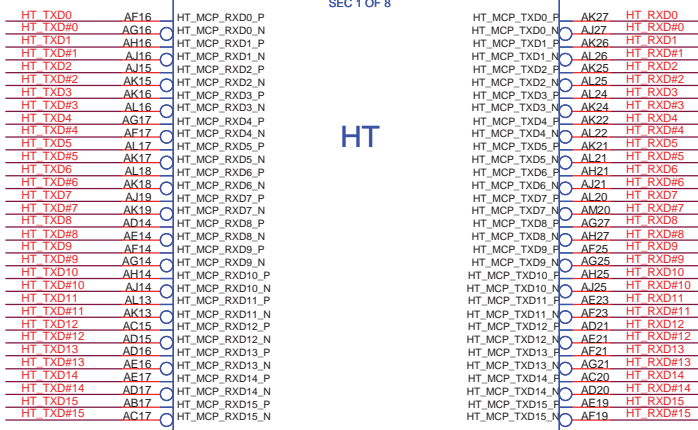
2 HT_TXD[15..0] HT_RXD[15..0] 2
 2 HT_TXD#1[15..0] HT_RXD#1[15..0] 2

A1:AJMCP670T00
 A2:AJMCP670T04

U24A
 FCBGA836-NVIDIA-MCP67

SEC 1 OF 8

HT



Quanta Computer Inc.
 PROJECT : ZY5D

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	MCP77 HyperTransport Bus	3B
Date:	Wednesday, May 21, 2008	Sheet 7 of 35

14 PEG_RXP[15:0] PEG_TXP[15:0] 14
 14 PEG_RXN[15:0] PEG_TXN[15:0] 14

U24B
 FCBGA836-NVIDIA-MCP67

SEC 2 OF 8

PEG_RXP0	F23	PE0_RX0_P
PEG_RXN0	G24	PE0_RX0_N
PEG_RXP1	F24	PE0_RX1_P
PEG_RXN1	F25	PE0_RX1_N
PEG_RXP2	D26	PE0_RX2_P
PEG_RXN2	D28	PE0_RX2_N
PEG_RXP3	C28	PE0_RX3_P
PEG_RXN3	D28	PE0_RX3_N
PEG_RXP4	C29	PE0_RX4_P
PEG_RXN4	C30	PE0_RX4_N
PEG_RXP5	D29	PE0_RX5_P
PEG_RXN5	D30	PE0_RX5_N
PEG_RXP6	F28	PE0_RX6_P
PEG_RXN6	F27	PE0_RX6_N
PEG_RXP7	F28	PE0_RX7_P
PEG_RXN7	F29	PE0_RX7_N
PEG_RXP8	H25	PE0_RX8_P
PEG_RXN8	H24	PE0_RX8_N
PEG_RXP9	H26	PE0_RX9_P
PEG_RXN9	H28	PE0_RX9_N
PEG_RXP10	H27	PE0_RX10_P
PEG_RXN10	H28	PE0_RX10_N
PEG_RXP11	K24	PE0_RX11_P
PEG_RXN11	K25	PE0_RX11_N
PEG_RXP12	K27	PE0_RX12_P
PEG_RXN12	K26	PE0_RX12_N
PEG_RXP13	K28	PE0_RX13_P
PEG_RXN13	K29	PE0_RX13_N
PEG_RXP14	J31	PE0_RX14_P
PEG_RXN14	J30	PE0_RX14_N
PEG_RXP15	K31	PE0_RX15_P
PEG_RXN15	K30	PE0_RX15_N

PCIE

Notice

Page 08 :
 MXM
 circuit
 ZY5D no
 use it

+3V_SS ○ R424 *10K 4 PCIE_WAKE#

Notice

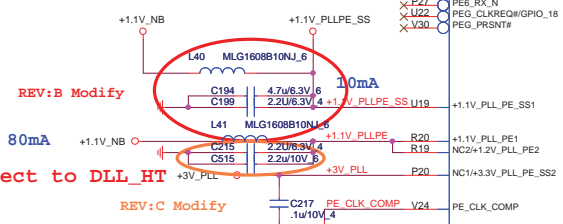
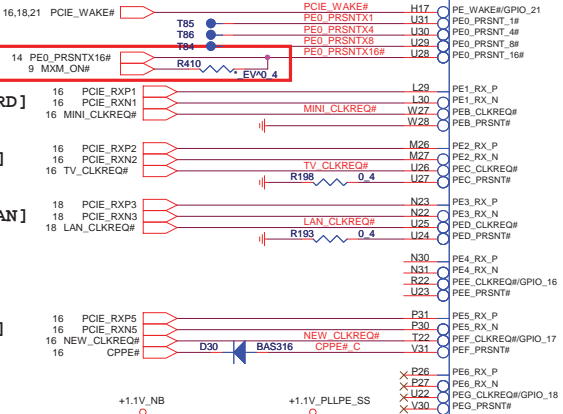
Page 08 : MXM circuit
 ZY5D no use it

[MINI CARD]

[TV]

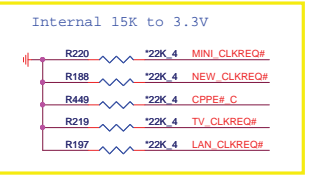
[Giga LAN]

[NEW CARD]



For EMI

CLK_PCIE_MXM	C316	*10P_4
CLK_PCIE_MXM#	C317	*10P_4
CLK_PCIE_MINI	C310	*10P_4
CLK_PCIE_MINI#	C309	*10P_4
CLK_PCIE_NEW_C	C297	*10P_4
CLK_PCIE_NEW_C#	C296	*10P_4
CLK_PCIE_LAN	C235	*10P_4
CLK_PCIE_LAN#	C245	*10P_4
CLK_PCIE_TV	C284	*10P_4
CLK_PCIE_TV#	C292	*10P_4



PE0_TX0_F	D24	C_PCIE_TXP0	C504	H-EVA1u10V#3	TXP0
PE0_TX0_N	C24	C_PCIE_TXP1	C506	H-EVA1u10V#3	TXN0
PE0_TX1_P	B24	C_PCIE_TXN1	C509	H-EVA1u10V#3	TXN1
PE0_TX2_P	B25	C_PCIE_TXP2	C510	H-EVA1u10V#3	TXP2
PE0_TX2_N	C25	C_PCIE_TXN2	C513	H-EVA1u10V#3	TXN2
PE0_TX3_P	B26	C_PCIE_TXP3	C514	H-EVA1u10V#3	TXP3
PE0_TX3_N	C26	C_PCIE_TXN3	C517	H-EVA1u10V#3	TXN3
PE0_TX4_P	D27	C_PCIE_TXN4	C519	H-EVA1u10V#3	TXN4
PE0_TX5_P	A28	C_PCIE_TXP5	C520	H-EVA1u10V#3	TXP5
PE0_TX5_N	B28	C_PCIE_TXN5	C521	H-EVA1u10V#3	TXN5
PE0_TX6_P	A29	C_PCIE_TXP6	C522	H-EVA1u10V#3	TXP6
PE0_TX6_N	B29	C_PCIE_TXN6	C524	H-EVA1u10V#3	TXN6
PE0_TX7_P	A30	C_PCIE_TXP7	C525	H-EVA1u10V#3	TXP7
PE0_TX7_N	B30	C_PCIE_TXN7	C529	H-EVA1u10V#3	TXN7
PE0_TX8_P	B31	C_PCIE_TXP8	C531	H-EVA1u10V#3	TXP8
PE0_TX8_N	B32	C_PCIE_TXN8	C536	H-EVA1u10V#3	TXN8
PE0_TX9_P	C31	C_PCIE_TXP9	C537	H-EVA1u10V#3	TXP9
PE0_TX9_N	C32	C_PCIE_TXN9	C541	H-EVA1u10V#3	TXN9
PE0_TX10_P	D31	C_PCIE_TXP10	C545	H-EVA1u10V#3	TXP10
PE0_TX10_N	D32	C_PCIE_TXN10	C547	H-EVA1u10V#3	TXN10
PE0_TX11_P	E31	C_PCIE_TXP11	C550	H-EVA1u10V#3	TXP11
PE0_TX11_N	E30	C_PCIE_TXN11	C551	H-EVA1u10V#3	TXN11
PE0_TX12_P	F31	C_PCIE_TXP12	C562	H-EVA1u10V#3	TXP12
PE0_TX12_N	F30	C_PCIE_TXN12	C564	H-EVA1u10V#3	TXN12
PE0_TX13_P	G29	C_PCIE_TXP13	C569	H-EVA1u10V#3	TXP13
PE0_TX13_N	G30	C_PCIE_TXN13	C561	H-EVA1u10V#3	TXN13
PE0_TX14_P	H29	C_PCIE_TXP14	C566	H-EVA1u10V#3	TXP14
PE0_TX14_N	H30	C_PCIE_TXN14	C567	H-EVA1u10V#3	TXN14
PE0_TX15_P	H32	C_PCIE_TXP15	C572	H-EVA1u10V#3	TXP15
PE0_TX15_N	H31	C_PCIE_TXN15	C574	H-EVA1u10V#3	TXN15

PEA_REFCLK_P R29 PED_REFCLK_P R216 *EV22_4
 PEB_REFCLK_N R30 PEB_REFCLK_N R217 *EV22_4

[MXM]

Notice

[MINI CARD ZY5 only]

[TV ZY5 only], MINI
 CARD ZY7 only]

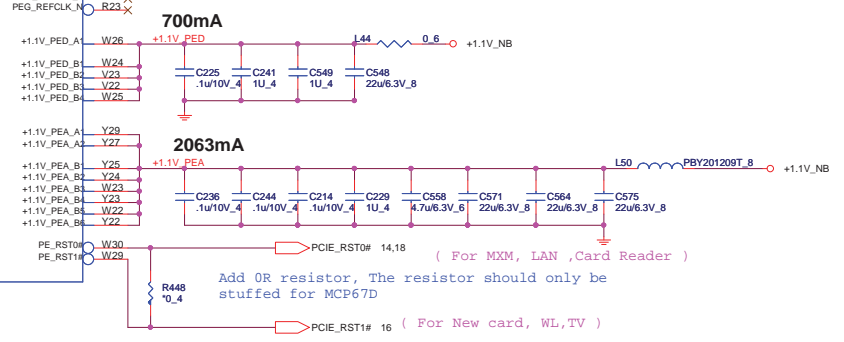
[Giga LAN]

ZY5D B modify use single stack_wireless Card
 [Card Reader] By Jack Weng

[NEW CARD]

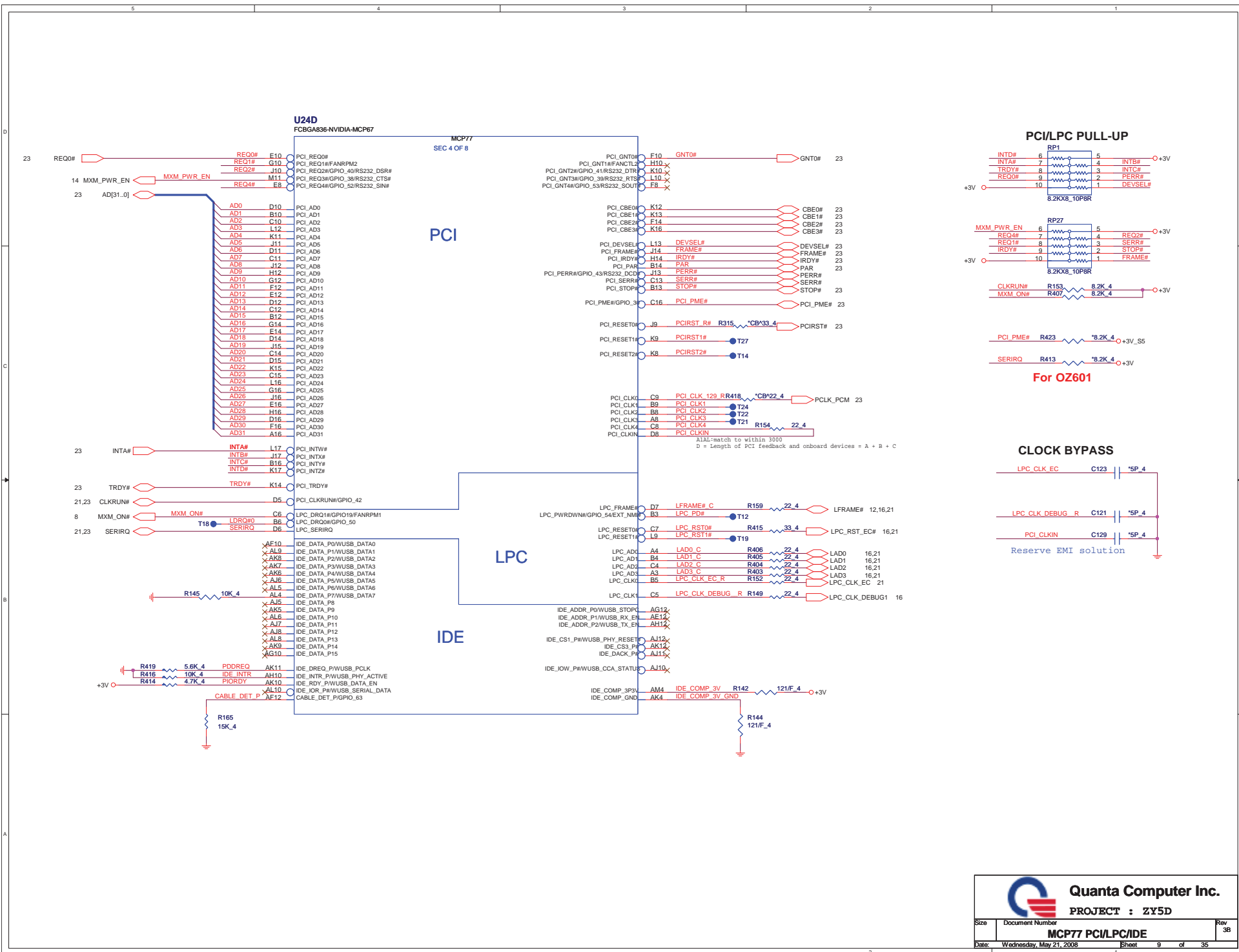
Page 08 : NEW CARD circuit
 ZY5D no use it


Notice



Quanta Computer Inc.
 PROJECT : ZY5D

Size	Document Number	Rev
	MCP77 PCI-Express Bus	38
Date: Friday, July 25, 2008	Sheet	8 of 35



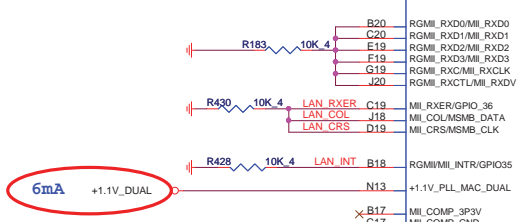


Quanta Computer Inc.
PROJECT : ZY5D

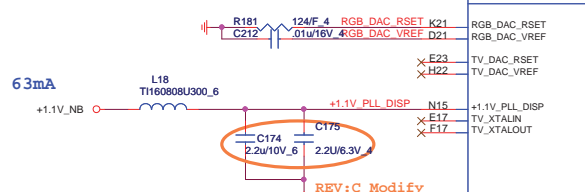
Size	Document Number	Rev
	MCP77 PCI/LPC/IDE	38
Date:	Wednesday, May 21, 2008	Sheet 9 of 35

U24C
FCBGA836-NVIDIA-MCP67

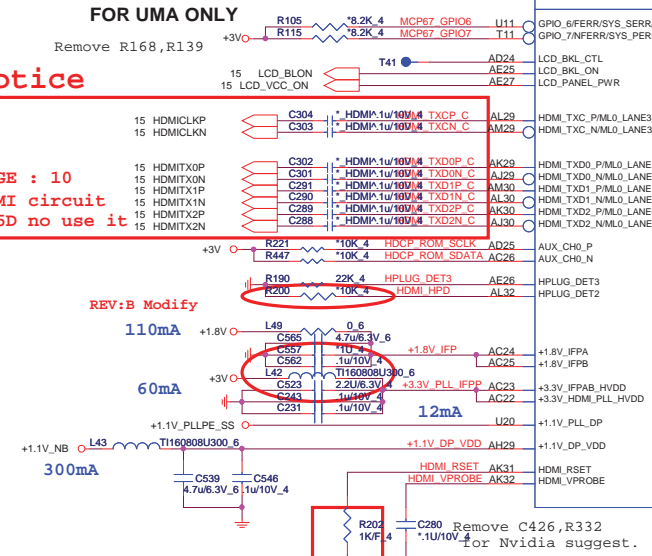
LAN



DACS



FLAT PANEL



Notice

PAGE : 10
HDMI circuit
ZY5D no use it

Notice

PAGE : 10
HDMI circuit
ZY5D no use it

9/17 NV FAE CHECK IT.

Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	MCP77 LAN and Graphics	3B
Date:	Wednesday, May 21, 2008	Sheet 10 of 35

U24E
FCBG836-NVIDIA-MCP67

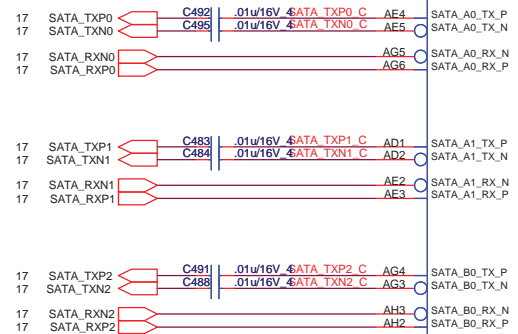
SEC 5 OF 8

[SATA HDD 1]

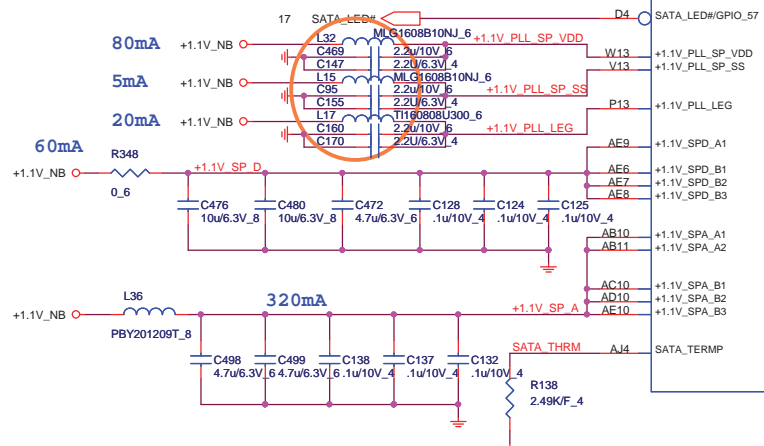
[SATA HDD 2]

[SATA ODD]

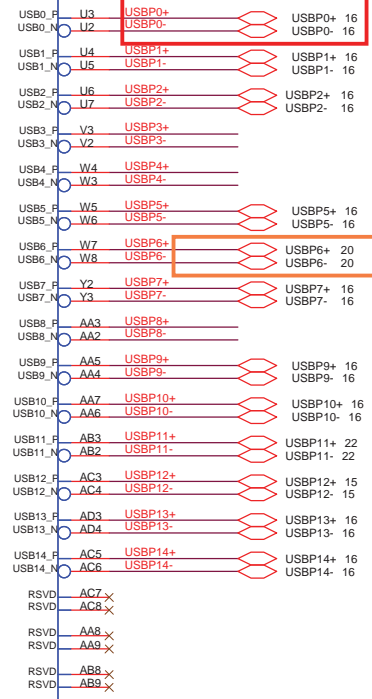
SATA USB



REV:C Modify



REV:B Modify



MINI CARD * 2

MINI CARD * 2

BLUETOOTH

REV:C Modify

INT LEFT USB 2

CARD READER

INT LEFT USB 1

Fingerprint

EXT USB * 2

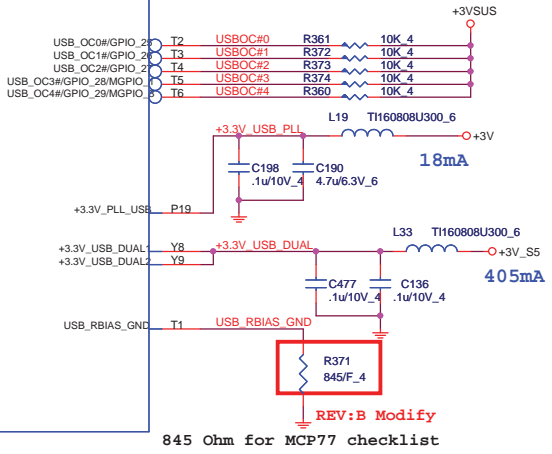
Docking

CCD

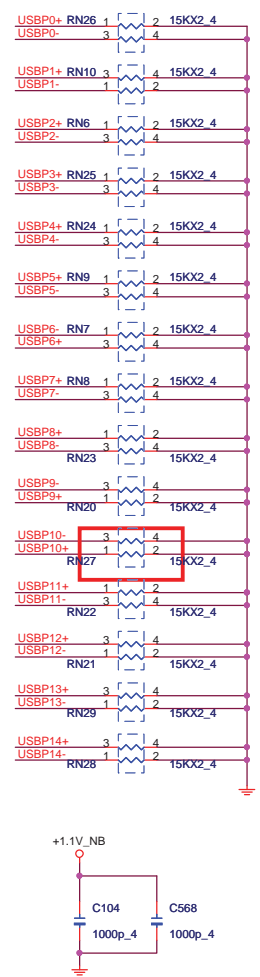
EXT USB * 2

NEW CARD

REV:B Swap Modify



USB PULL-DOWN



Quanta Computer Inc.
 PROJECT : ZY5D

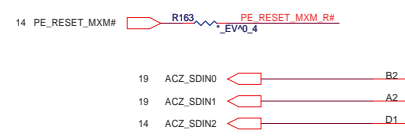
Size	Document Number	Rev
	MCP77 SATA and USB	3B
Date:	Wednesday, May 21, 2008	Sheet 11 of 35

U24F
FCBGA836-NVIDIA-MCP67

SEC 6 OF 8

HDA

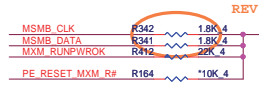
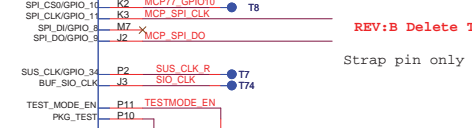
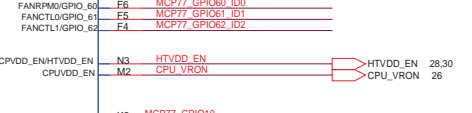
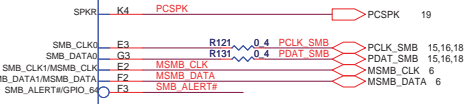
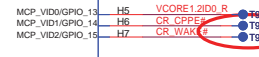
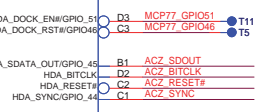
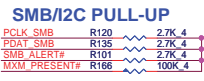
MISC



MXM_RUNPWROK need to Connect from MXM card



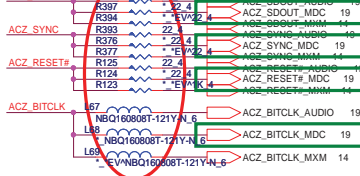
Delay 10ms after S5 powerOK



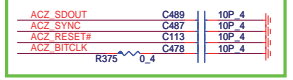
??? CHECK MB ID
M/B ID for 14"/17"

ID0	ID1	ID2	M/B
0	0	0	1.7" D
0	0	1	X
0	1	0	1.5" D
1	0	0	1.5" U
1	0	1	1.4" Dual Core CPU & MXM
1	1	0	1.4" Dual Core CPU & UMA
1	1	1	1.4" Single Core CPU & UMA

HDA ZY5D B TEST DEL MODEM BY JACK WENG



REV:E Modify by NV



REV:C Modify

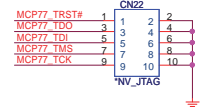
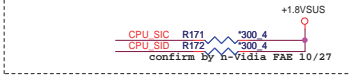
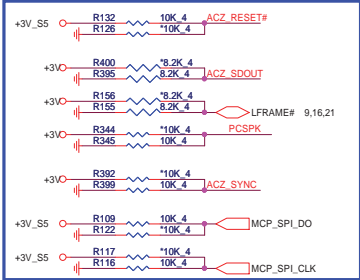
REV:B Delete T20

Strap pin only

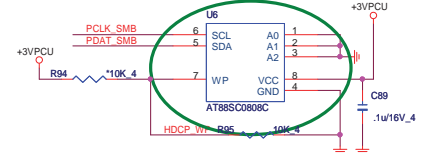
REV:C Modify

STRAPPING

Pin	Value	Default
HDA RESETA (LAN)	0	MII
HDA_SDOUT_R_LFRAME# (BIOS)	1	RGMII (DEFAULT)
HDA_SDOUT_R_LFRAME# (BIOS)	10	SPI BIOS
HDA_SDOUT_R_LFRAME# (BIOS)	11	RESERVED (SPI)
MCP_SPKR (Bos MODE)	0	USER TABLE (DEFAULT)
MCP_SPKR (Bos MODE)	1	SAFE TABLE
HDA_SYNC_R (SIO CLOCK)	0	14.318MHz (DEFAULT)
HDA_SYNC_R (SIO CLOCK)	1	24MHz
SPI_DO_SPL_CLK (SPL CLOCK)	00	31MHz
SPI_DO_SPL_CLK (SPL CLOCK)	01	42MHz
SPI_DO_SPL_CLK (SPL CLOCK)	10	52MHz
SPI_DO_SPL_CLK (SPL CLOCK)	11	1MHz



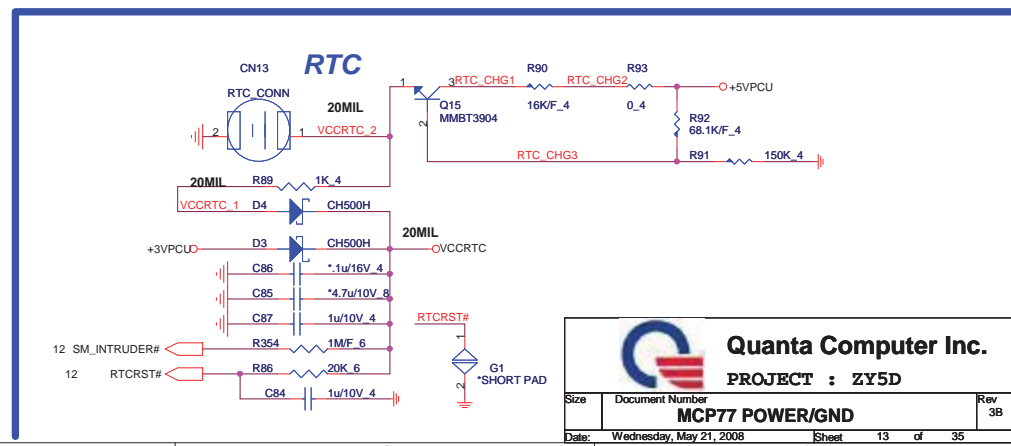
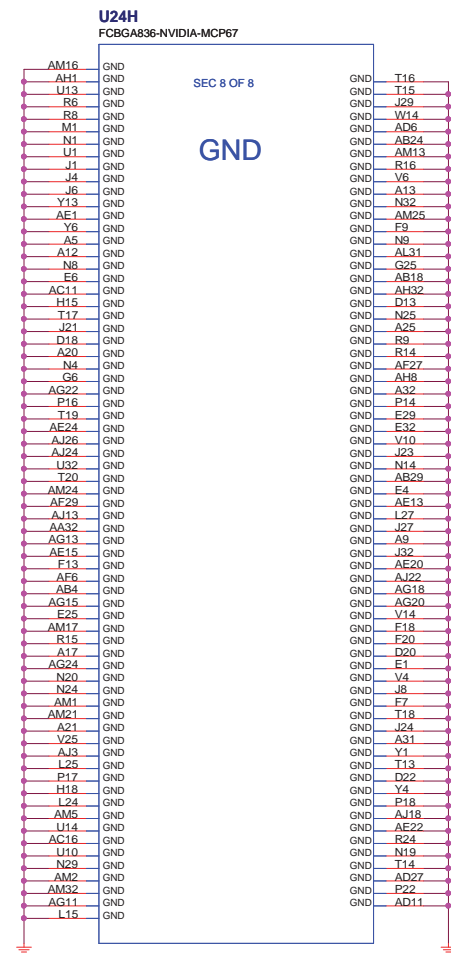
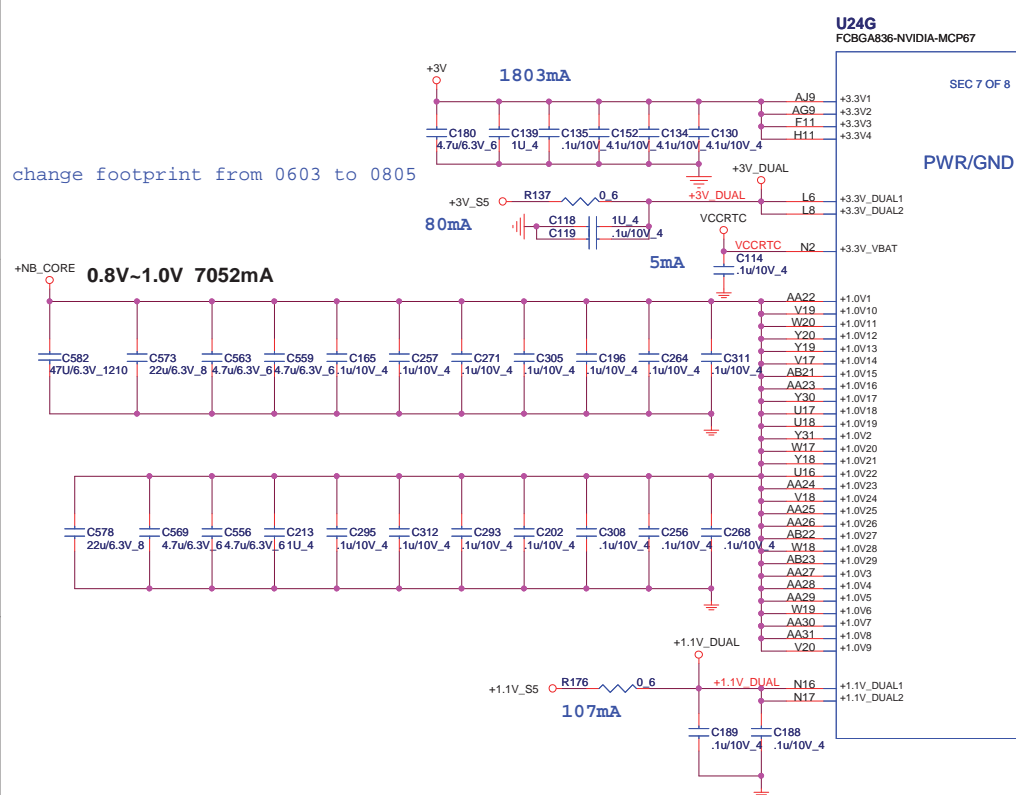
HDCP 2-WIRE ROM ZY5D B Modify By Jack Weng



C3A:BCZ timing issue, modify to 22P

B2B: CHANGED CAP FROM 0.1U TO 1U FOR DELAY HT_VLD

MCP77 POWER PLANE/GND & BYPASS



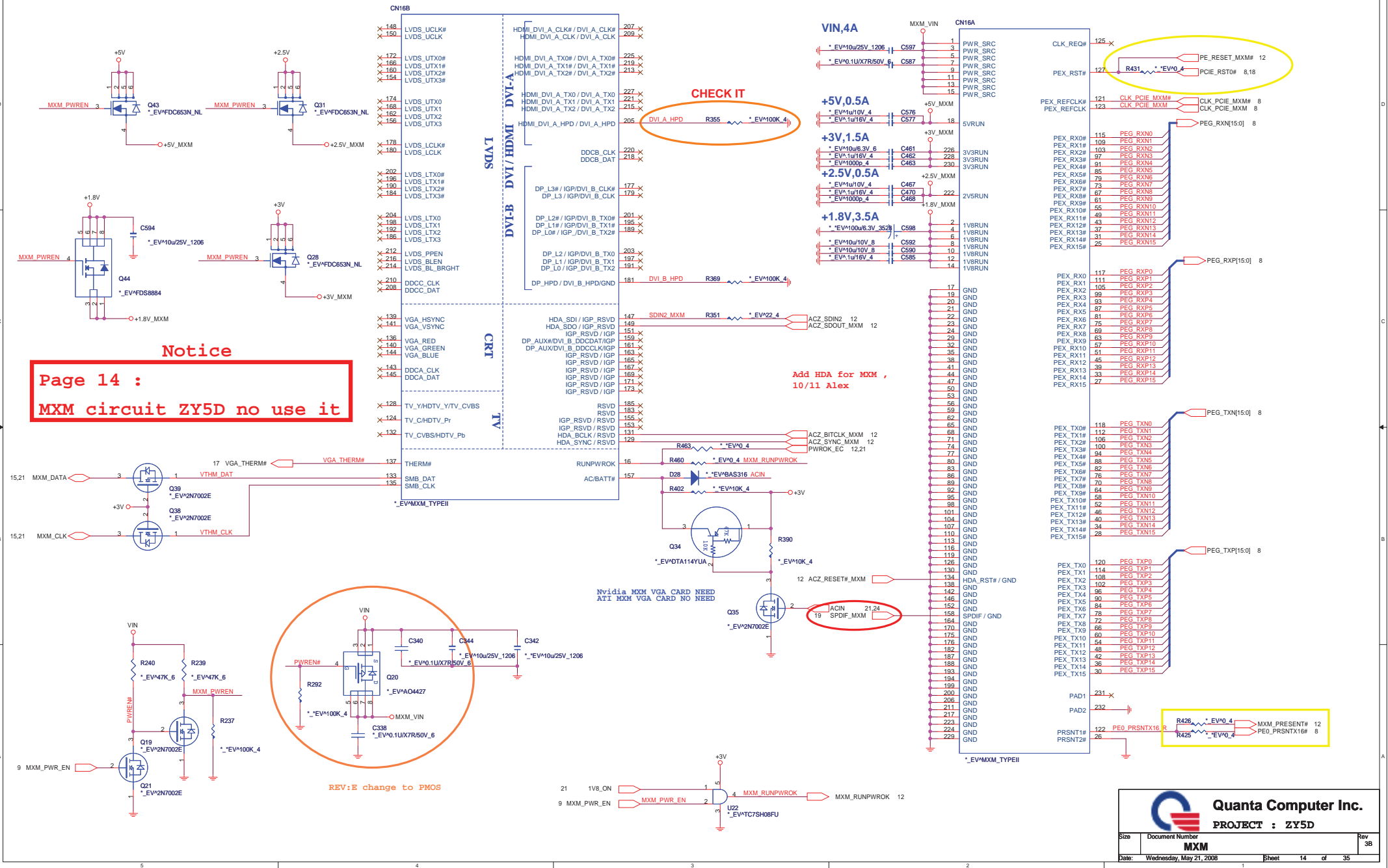
Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	MCP77 POWER/GND	3B
Date: Wednesday, May 21, 2008		Sheet 13 of 35

Notice

Page 14 :

MXM circuit ZY5D no use it



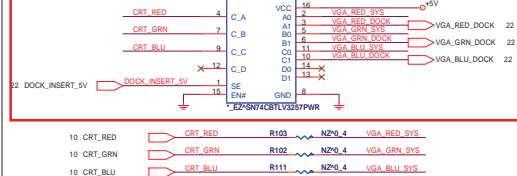
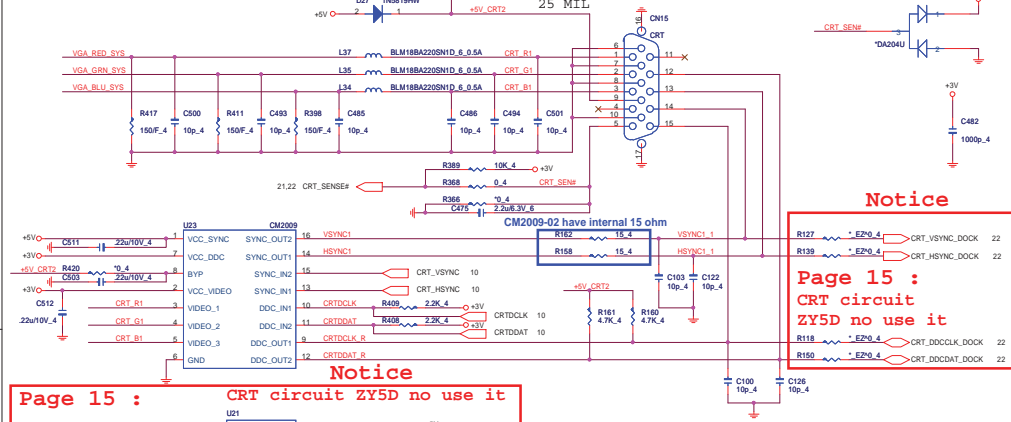
Quanta Computer Inc.

PROJECT : ZY5D

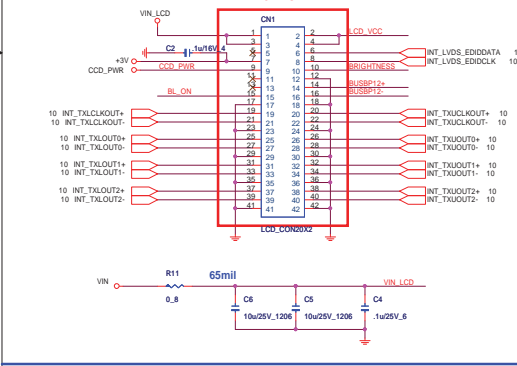
Size	Document Number	Rev
	MXM	38

Date: Wednesday, May 21, 2008 Sheet 14 of 35

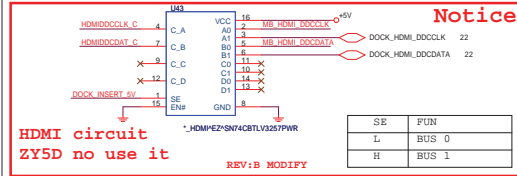
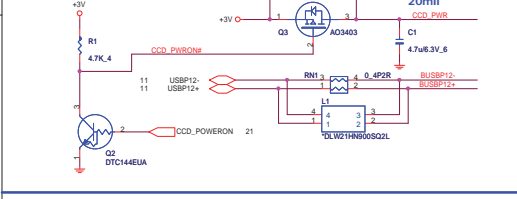
CRT



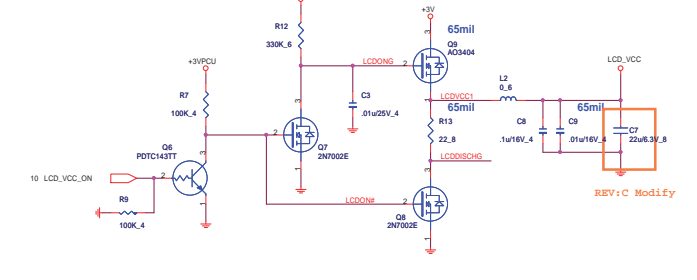
LVDS



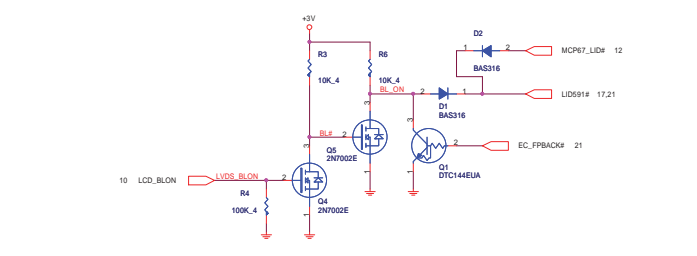
Camera



LCD_ON



Backlight Control



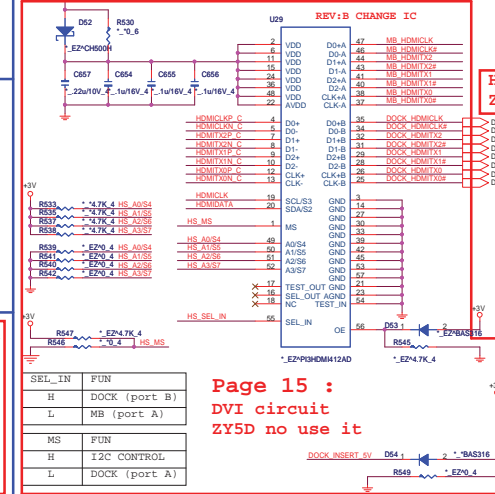
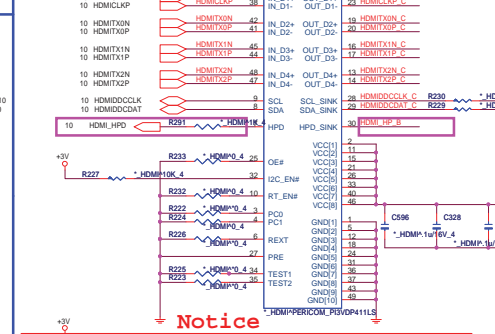
BRIGHTNESS



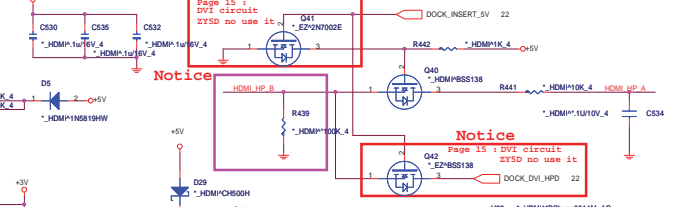
LCD EDID SMBus PU



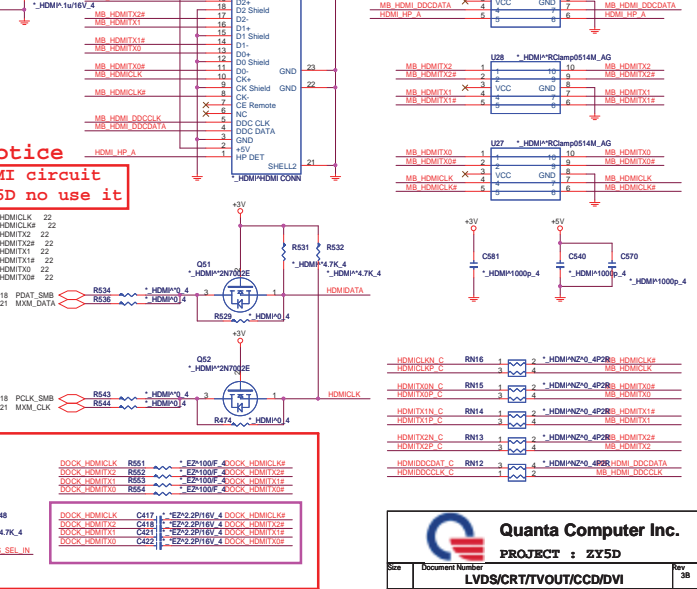
HDMI



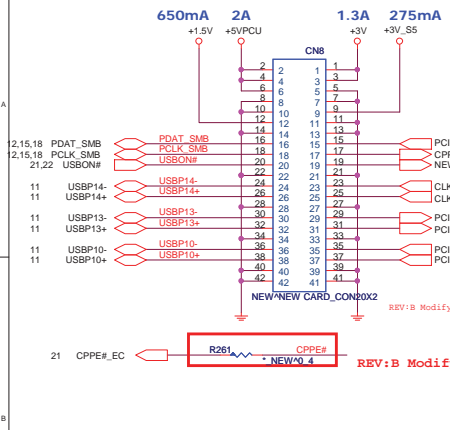
DVI



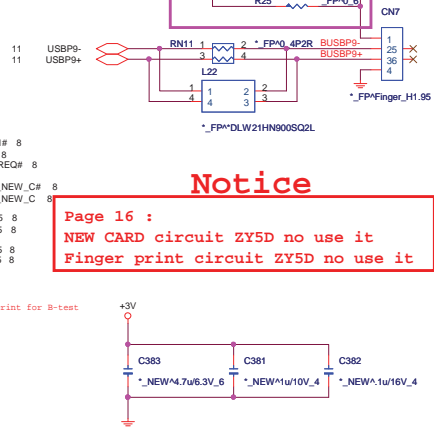
HDMI circuit



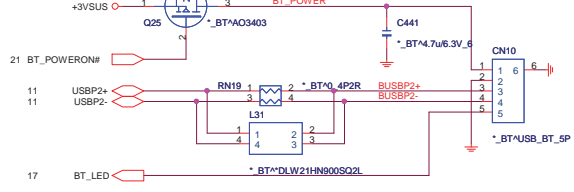
To NEW-CARD & EXT. USB



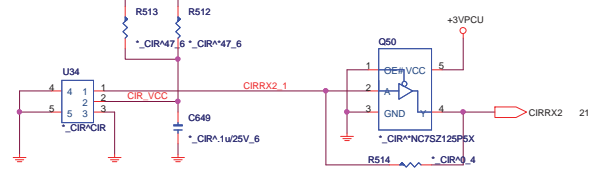
Fingerprint



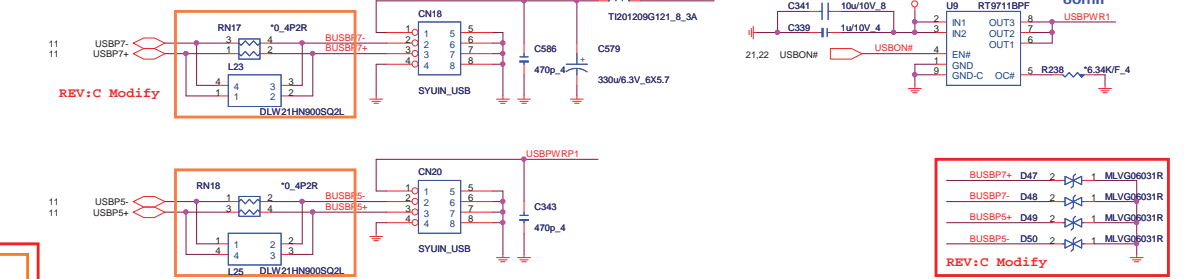
Bluetooth



CIR

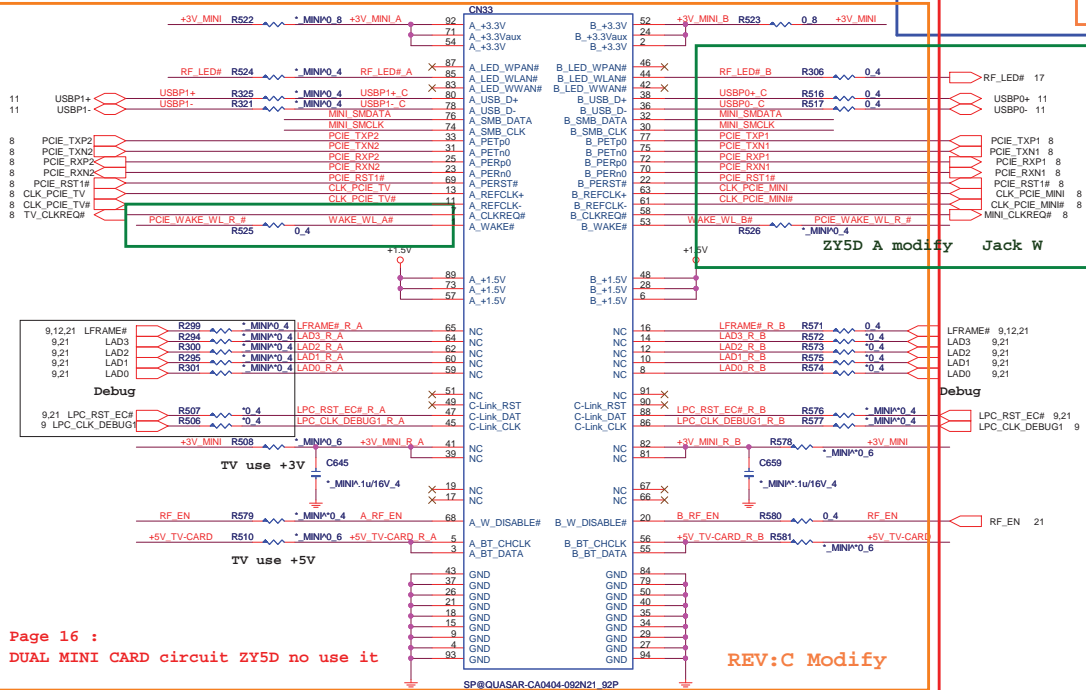


INT. USB

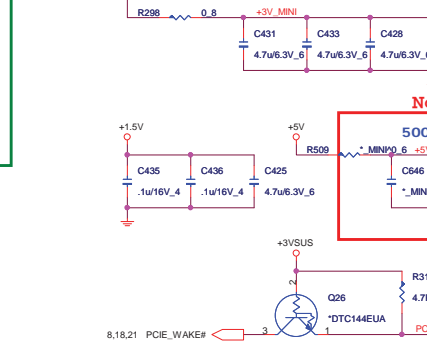


MINI-CARD

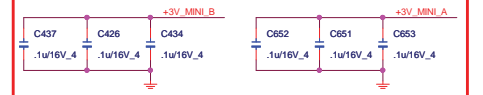
Notice



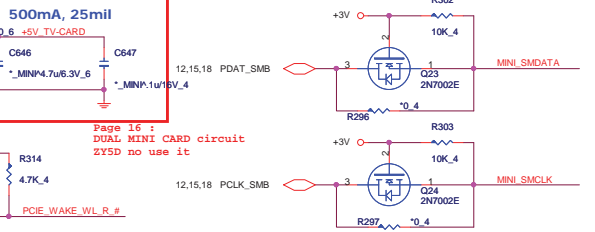
+3V for WWAN card is 2.75A



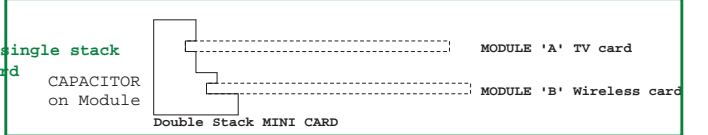
REV:B Modify



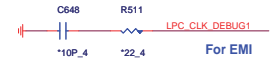
Notice



ZY5D B test has modified to single stack
no TV card, only Wireless card



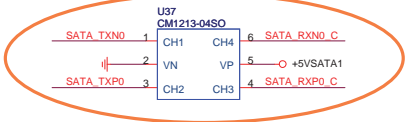
Page 16 :
DUAL MINI CARD circuit ZY5D no use it



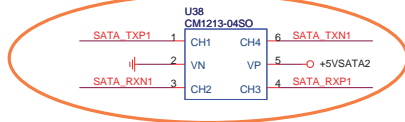
Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number	Rev
	NEW&MINI&TV CARD/USB/BT/CIR	38
Date: Thursday, July 24, 2008	Sheet	16 of 35

SATA1

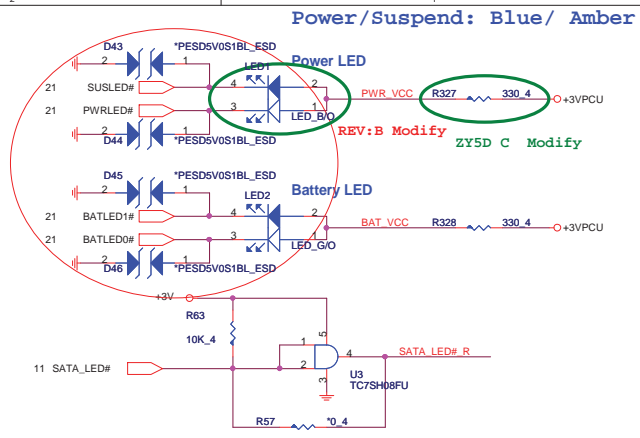


SATA2



REV:E add ESD

LED

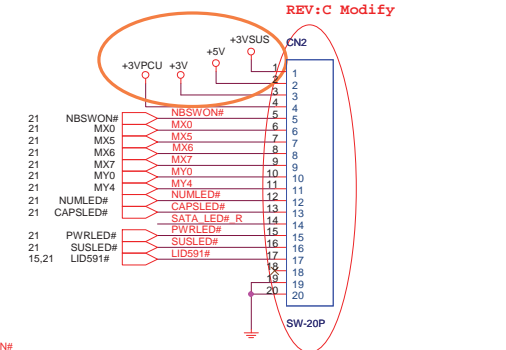


Power/Suspend: Blue/ Amber

REV:B Modify

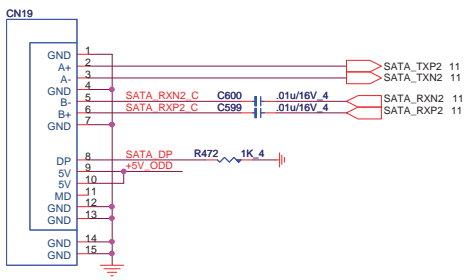
ZY5D C Modify

To Power/B

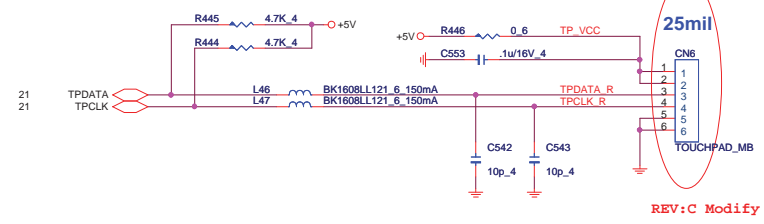


REV:C Modify

ODD (SATA)



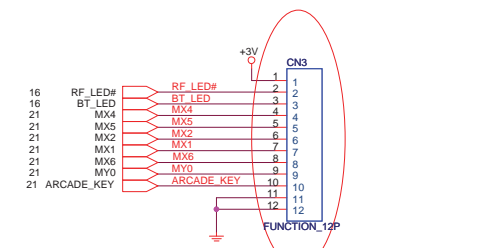
TP CONN



REV:C Modify

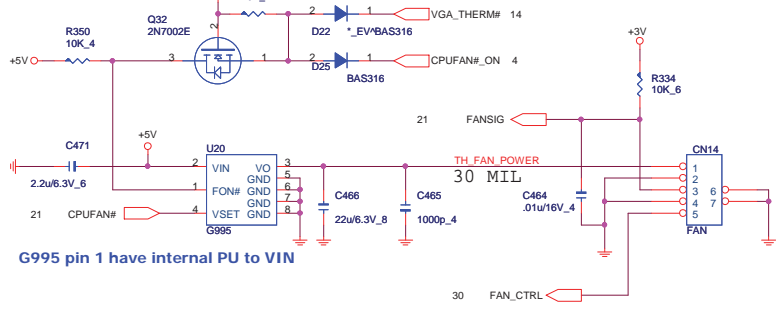
REV:B Modify

To Switch/B




REV:C Modify

FAN



G995 pin 1 have internal PU to VIN

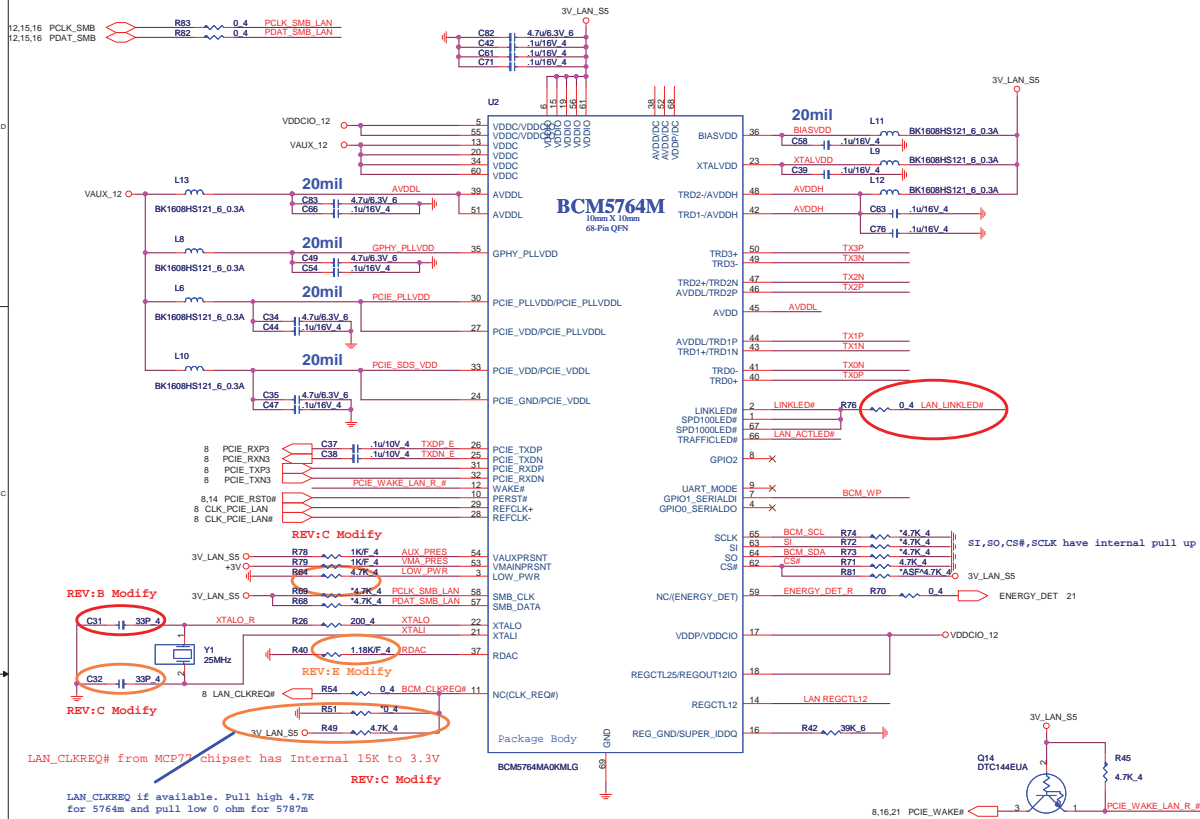
REV:E add ESD



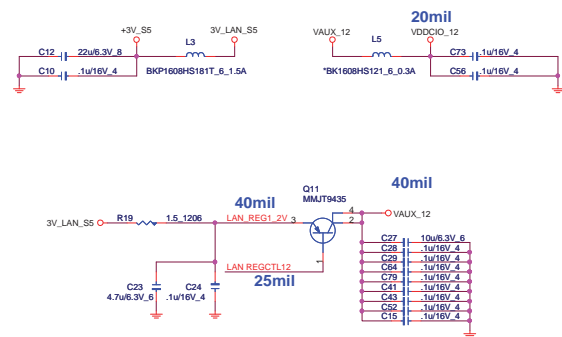
Quanta Computer Inc.
PROJECT : ZY5D

Size	Document Number HDD/ODD/LED/SW/TP/FAN	Rev 3B
Date:	Friday, July 25, 2008	Sheet 17 of 35

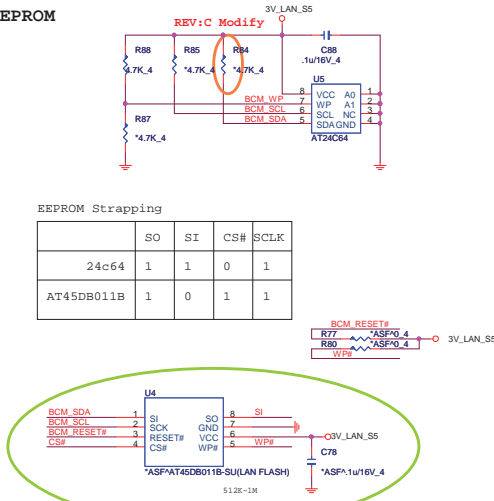
Giga LAN BCM5787M/5764M



LAN POWER

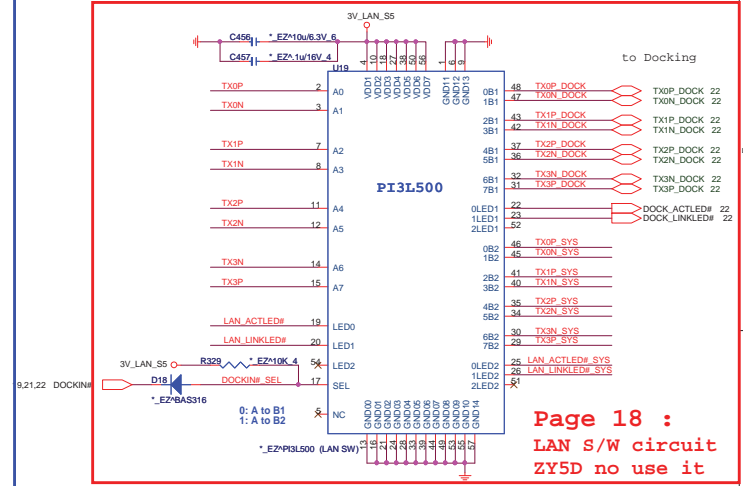


EEPROM



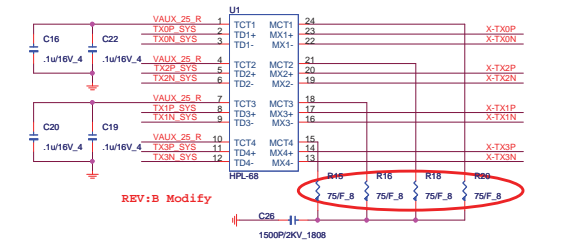
LAN SWITCH

Notice

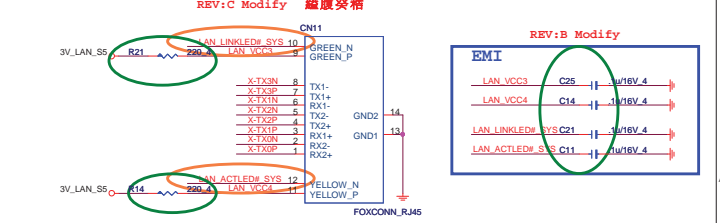


Transformer

Source 1: DELTA LFE9249 DBOZR1LAN11
 Source 2: Bothand GST5009 DBKN1NLAN03



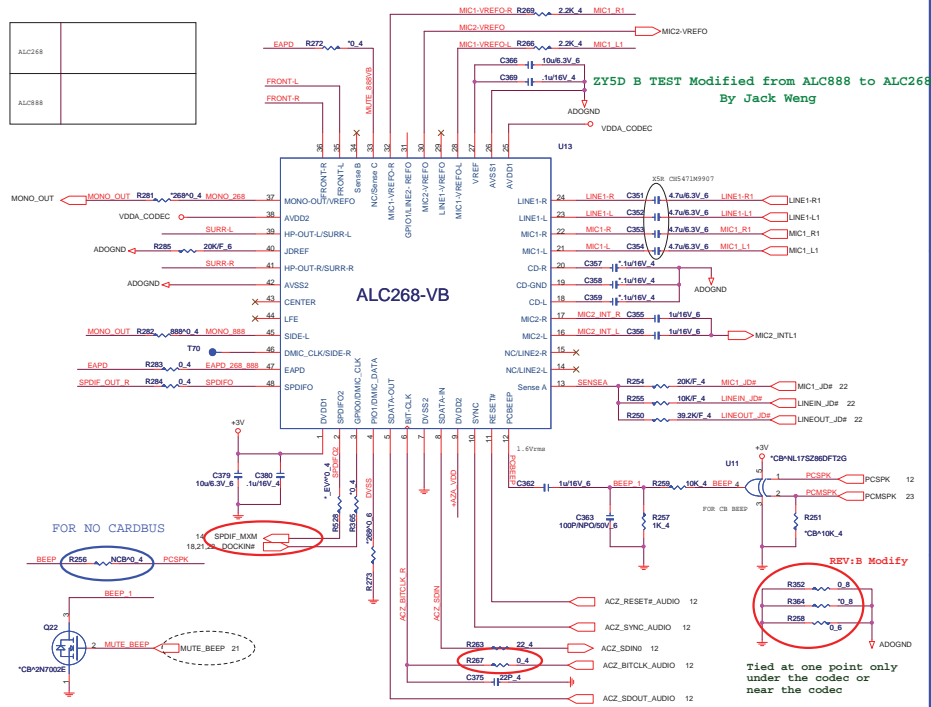
RJ45 connector



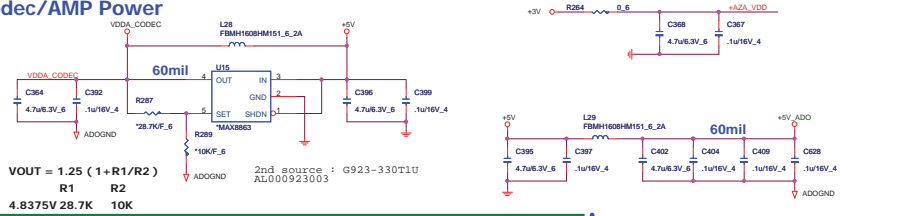
ZY5D C TEST Modified footprint from 0402 to 0805 to solve Lan burnt issue on Acer project

By Jack Weng

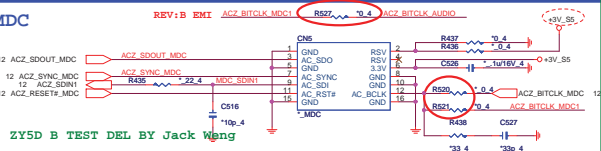
CODEC



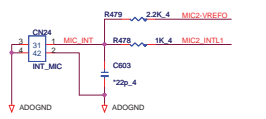
Codec/AMP Power



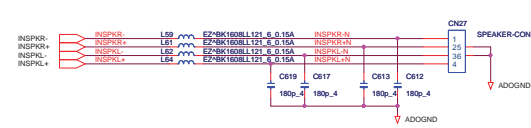
MDC



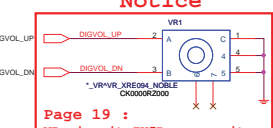
INT MIC.



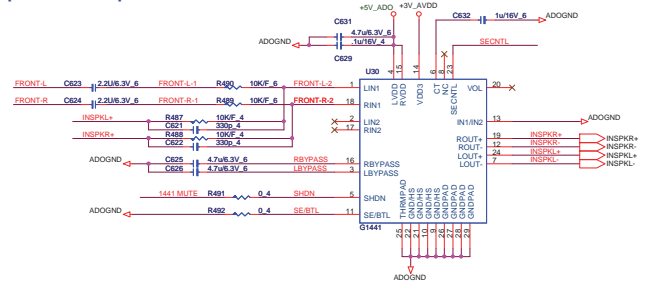
SPEAKER



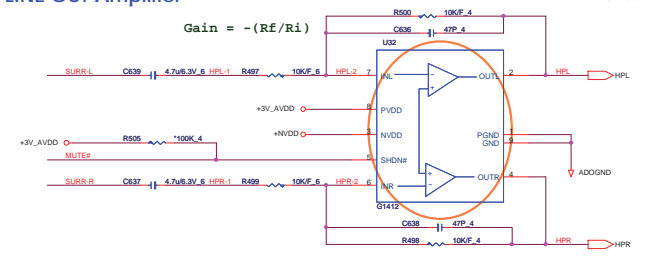
VR



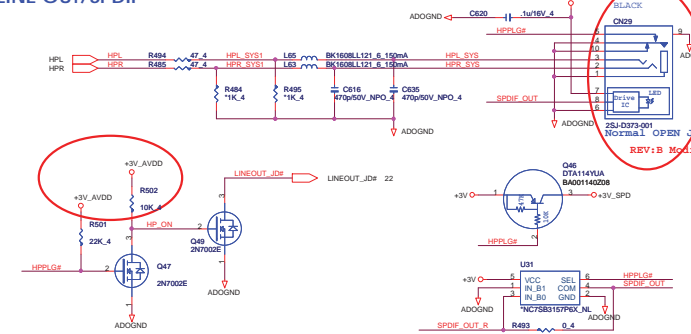
Speaker Amplifier



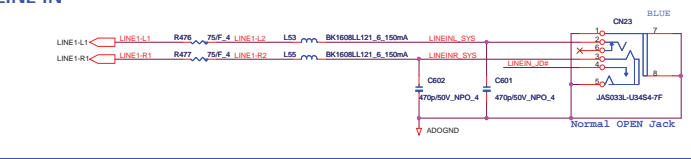
LINE OUT Amplifier



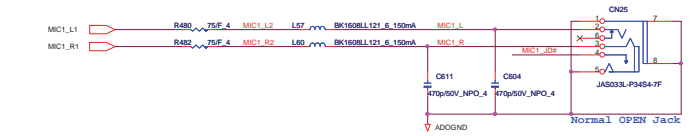
LINE OUT/SPDIF



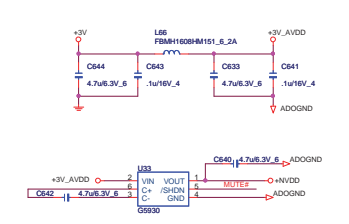
LINE IN



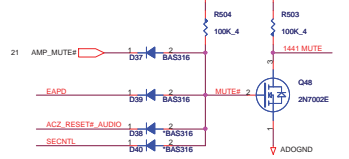
MIC



Amplifier POWER



MUTE



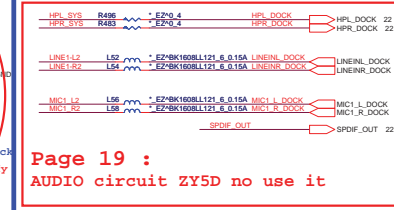
SUBWOOFER

Notice

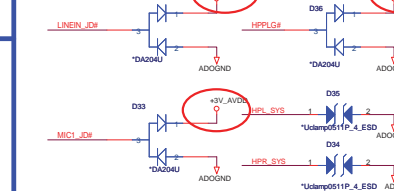


TO DOCKING

Notice



ESD



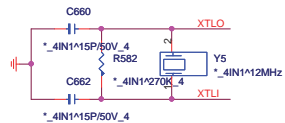
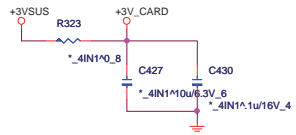
Quanta Computer Inc.

PROJECT : ZYSD

Doc. Number: **CODEC/AMP/MDC**

Rev: **30**

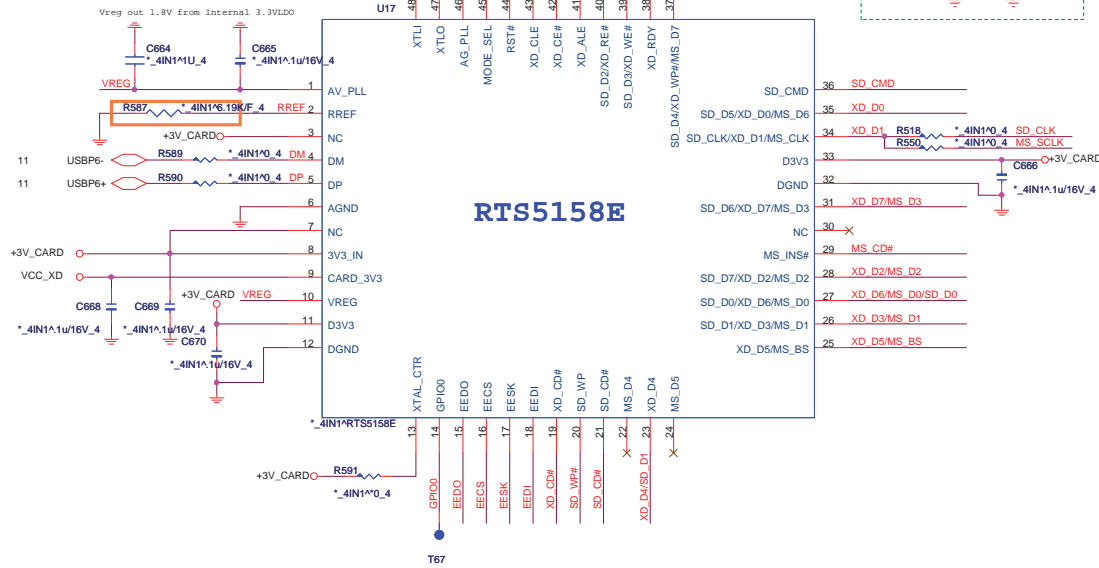
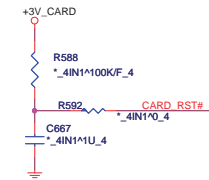
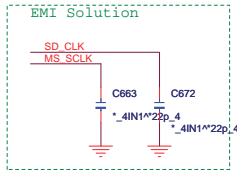
Date: Thursday, July 25, 2008 Sheet: 19 of 39



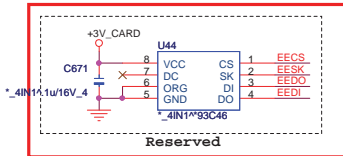
R583/C661 = 10K/47pF => R584 Reside
R583/C661 = NC / NC => R585 Reside

Notice

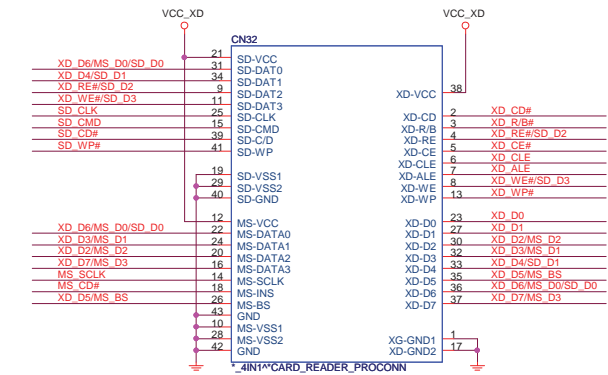
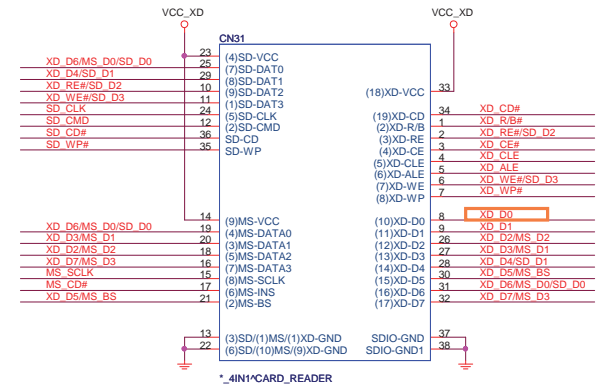
Page 20 :
4 IN 1 CARD READER circuit ZY5D no use it



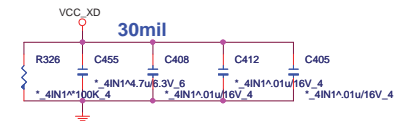
EEPROM



4 IN 1 CARD READER



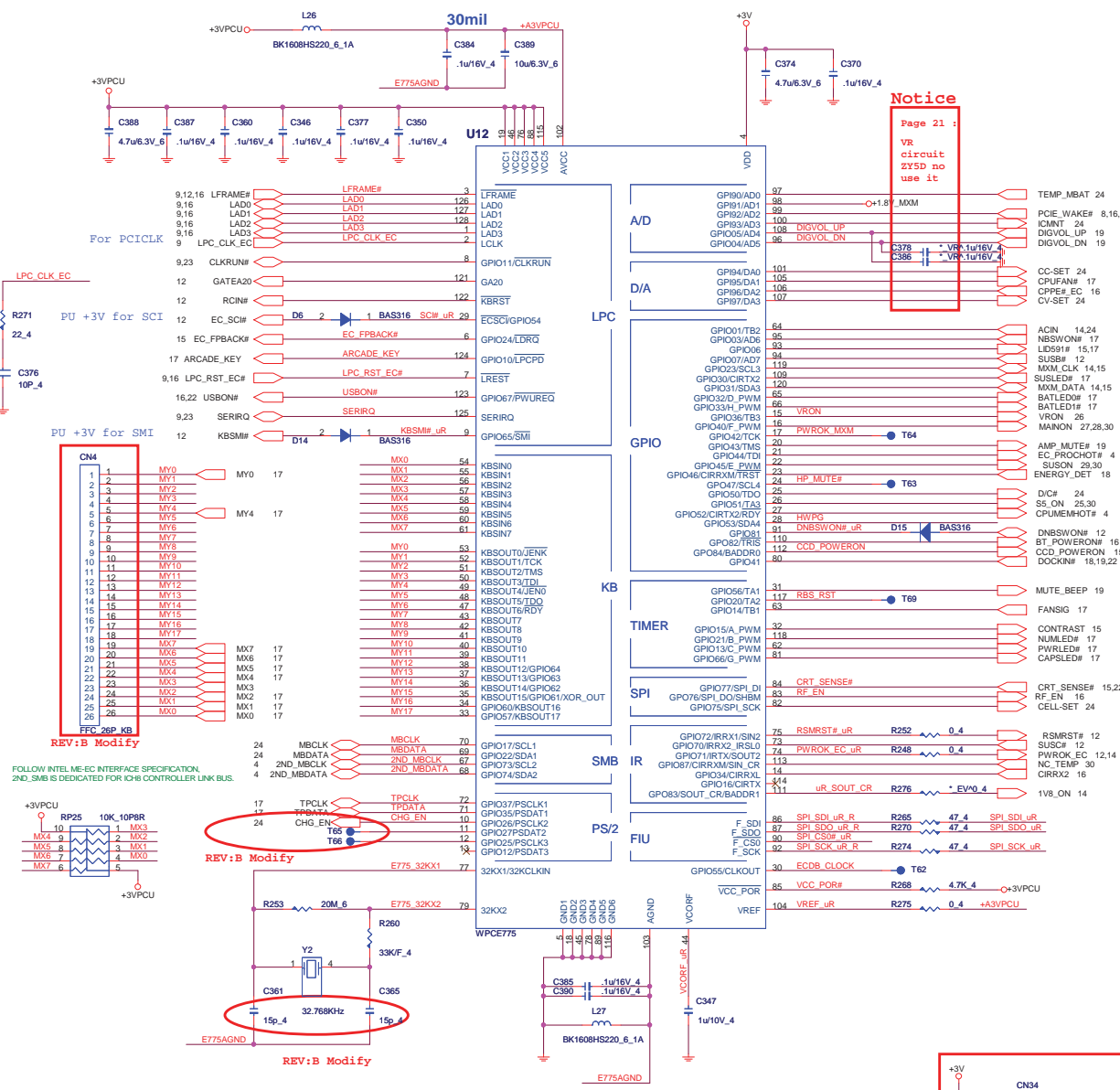
CARDREADER POWER



Quanta Computer Inc.

PROJECT : ZY5D

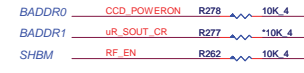
Size	Document Number	Rev
	CARD READER RTS5158E	3B
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I/O ADDRESS SETTING

I/O Address	
BADDR1-0	Index Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

SHBM=0: Enable shared memory with host BIOS



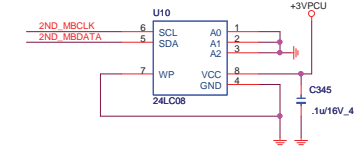
1/13 Confirm by vendor mail :
Disabled (*) if using FWH device on LPC.
Enabled (0) if using SPI flash for both system BIOS and EC firmware

SM BUS PU

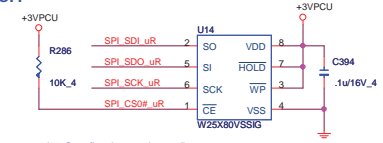


REV:B Modify

ACER ID

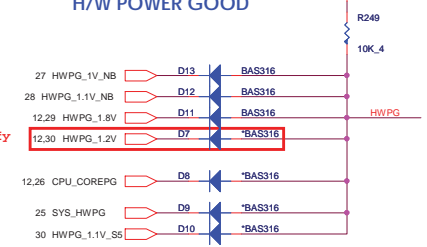


SPI FLASH



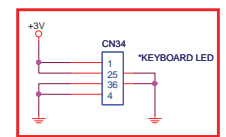
1/13 Confirm by vendor mail :
If the Southbridge enables Long Wait Abort by default, the flash device should be 50MHz (or faster)

H/W POWER GOOD



REV:B Modify

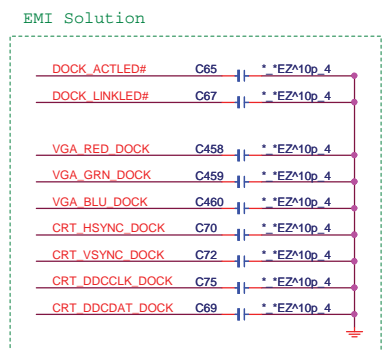
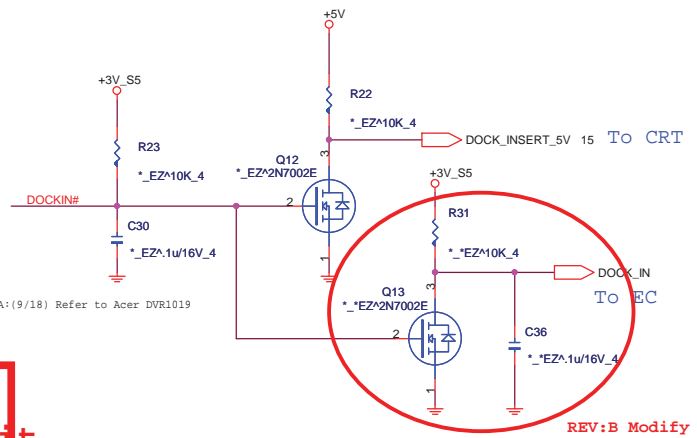
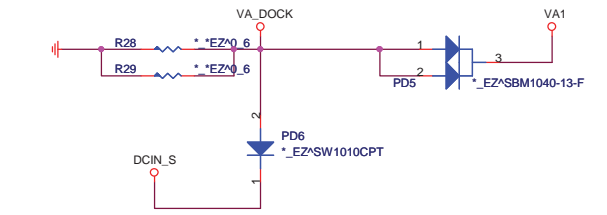
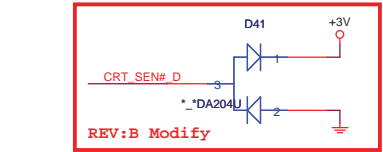
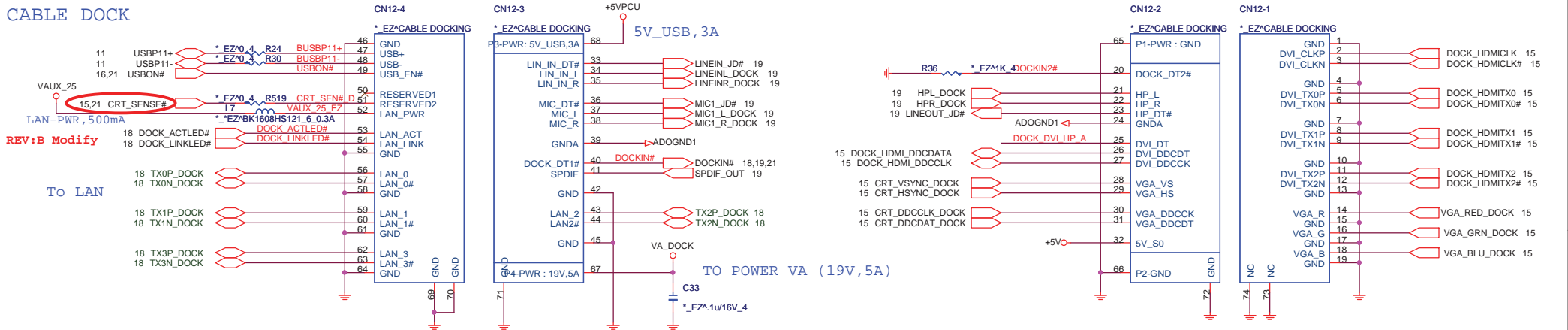
INTERNAL KEYBOARD STRIP SET



REV:B Modify

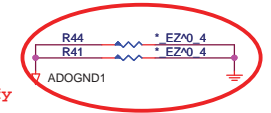
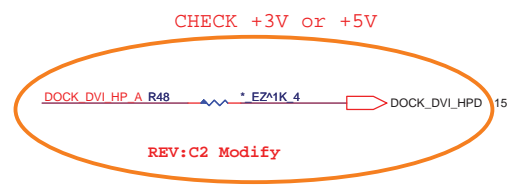
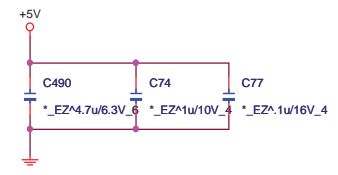
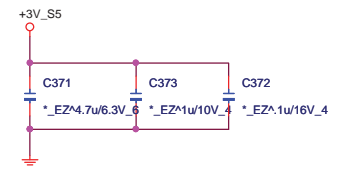
08/10 FAE
L43 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.

CABLE DOCK



Notice

Page 22 : CABLE DOCK circuit ZY5D no use it



Quanta Computer Inc.

PROJECT : ZY5D

Size	Document Number	Rev
	CABLE DOCK	3B
Date:	Wednesday, May 21, 2008	Sheet 22 of 35

NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

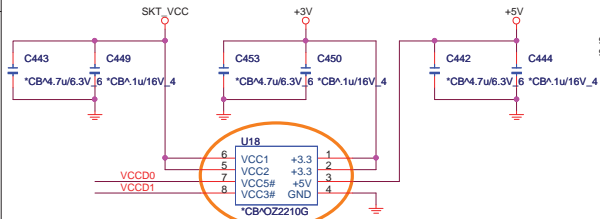
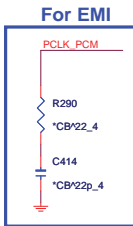
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

AD20 R309 *CB*100F_4 PCM IDSEL

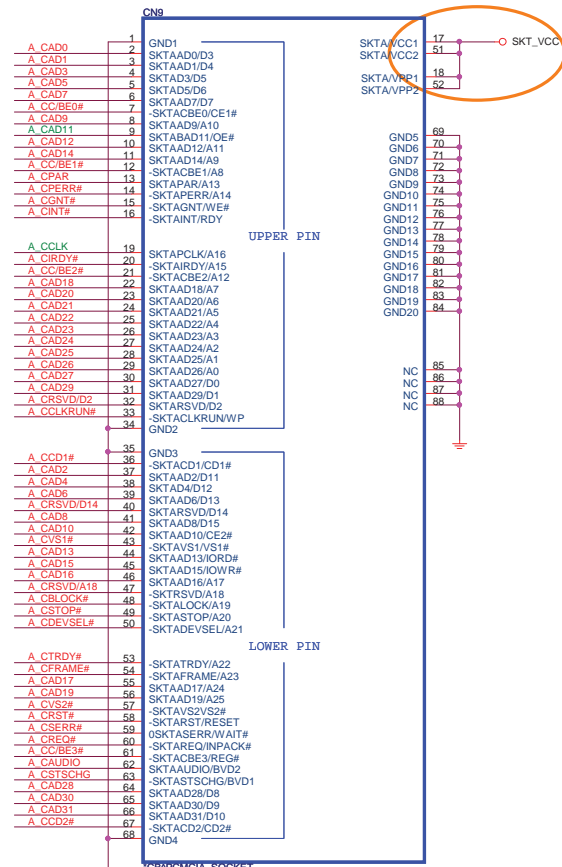
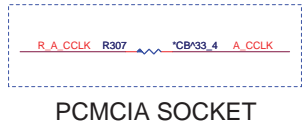
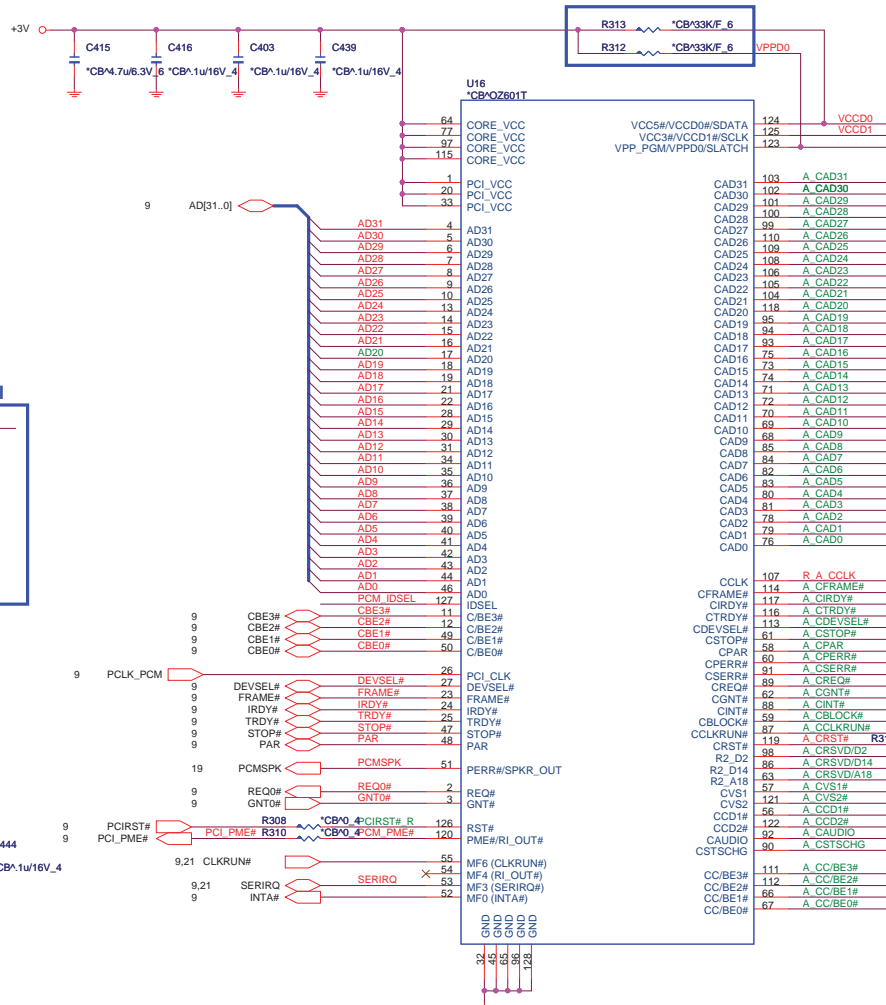
ID Select : AD20
 Interrupt Pin : INTA#
 Request Indicate : REQ0#
 Grant Indicate : GNT0#



Check Footprint & P/N

22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

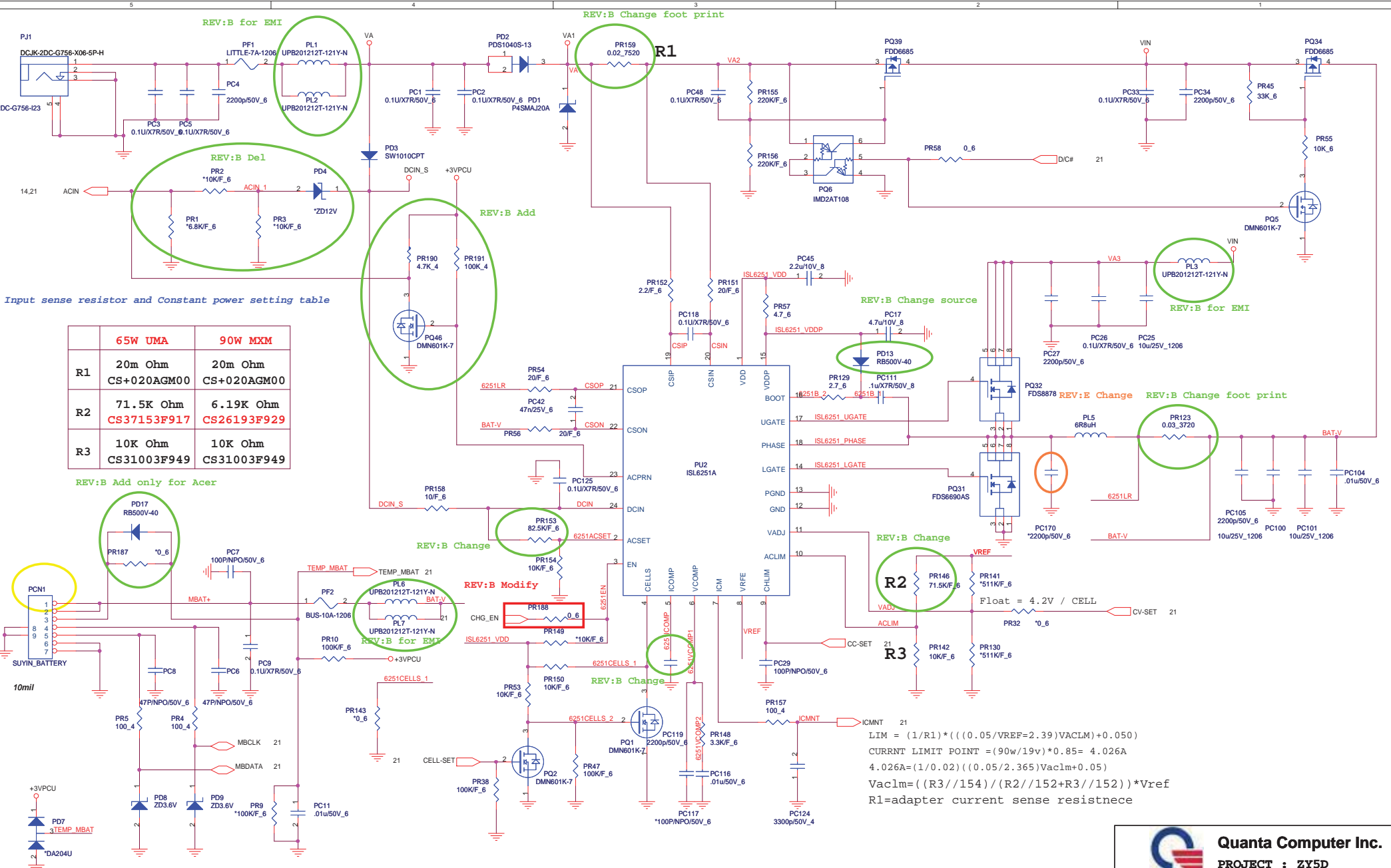
IDSEL SELECT POWER-ON-STRAPPING (SEE NOTE & TABLE FOR OPTIONS)



Check it

Quanta Computer Inc.
PROJECT : ZY5D

Size Document Number
PCMCIA(OZ601)
 Date: Wednesday, May 21, 2008 Sheet 23 of 35 Rev 3B



Input sense resistor and Constant power setting table

	65W UMA	90W MXM
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	71.5K Ohm CS37153F917	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949

REV:B Add only for Acer

$$LIM = (1/R1) * (((0.05/VREF=2.39)VACLIM)+0.050)$$

$$CURRNT LIMIT POINT = (90w/19v) * 0.85 = 4.026A$$

$$4.026A = (1/0.02) * (((0.05/2.365)VacLim+0.05)$$

$$VacLim = ((R3//154)/(R2//152+R3//152)) * Vref$$

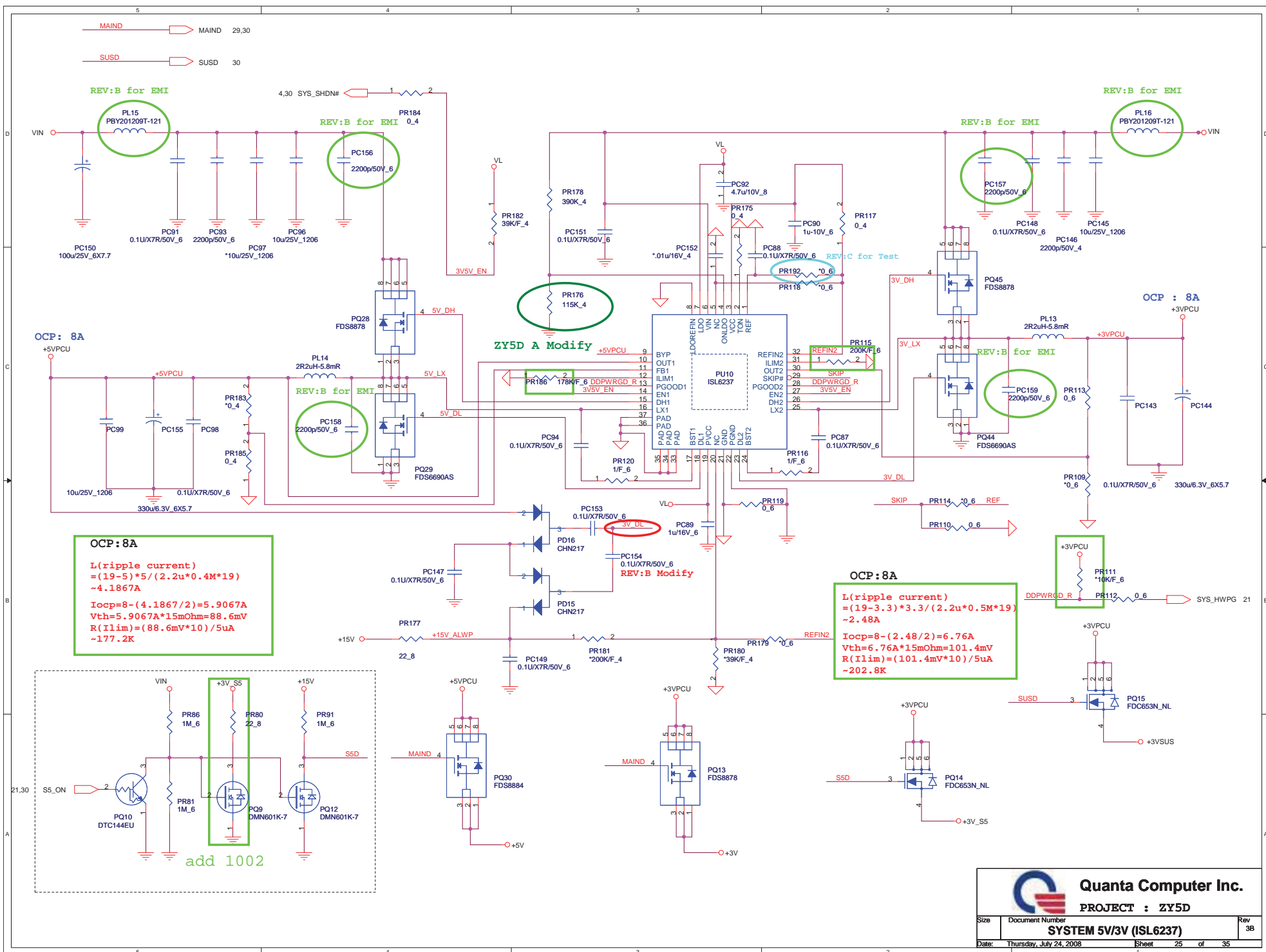
R1=adapter current sense resistence

CELL-SET = Hi ----> Cells = VDD ----> 4S
 CELL-SET = Low ----> Cells = GND ----> 3S

A: (9/7) Add ESD diode base on EC FAE suggestion

Quanta Computer Inc.
 PROJECT : ZYS9
CHARGER (ISL6251A)
 Date: Wednesday, May 21, 2008 Sheet 24 of 35

Size Document Number Rev 3B

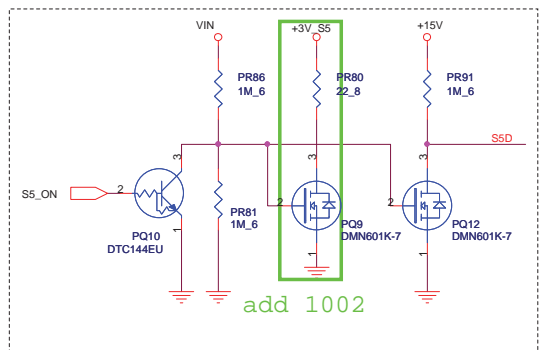


OCP: 8A

$L(\text{ripple current}) = (19-5) * 5 / (2.2u * 0.4m * 19) \sim 4.1867A$
 $I_{ocp} = 8 - (4.1867 / 2) = 5.9067A$
 $V_{th} = 5.9067A * 15m\Omega = 88.6mV$
 $R(I_{lim}) = (88.6mV * 10) / 5uA \sim 177.2K$

OCP: 8A

$L(\text{ripple current}) = (19-3.3) * 3.3 / (2.2u * 0.5m * 19) \sim 2.48A$
 $I_{ocp} = 8 - (2.48 / 2) = 6.76A$
 $V_{th} = 6.76A * 15m\Omega = 101.4mV$
 $R(I_{lim}) = (101.4mV * 10) / 5uA \sim 202.8K$



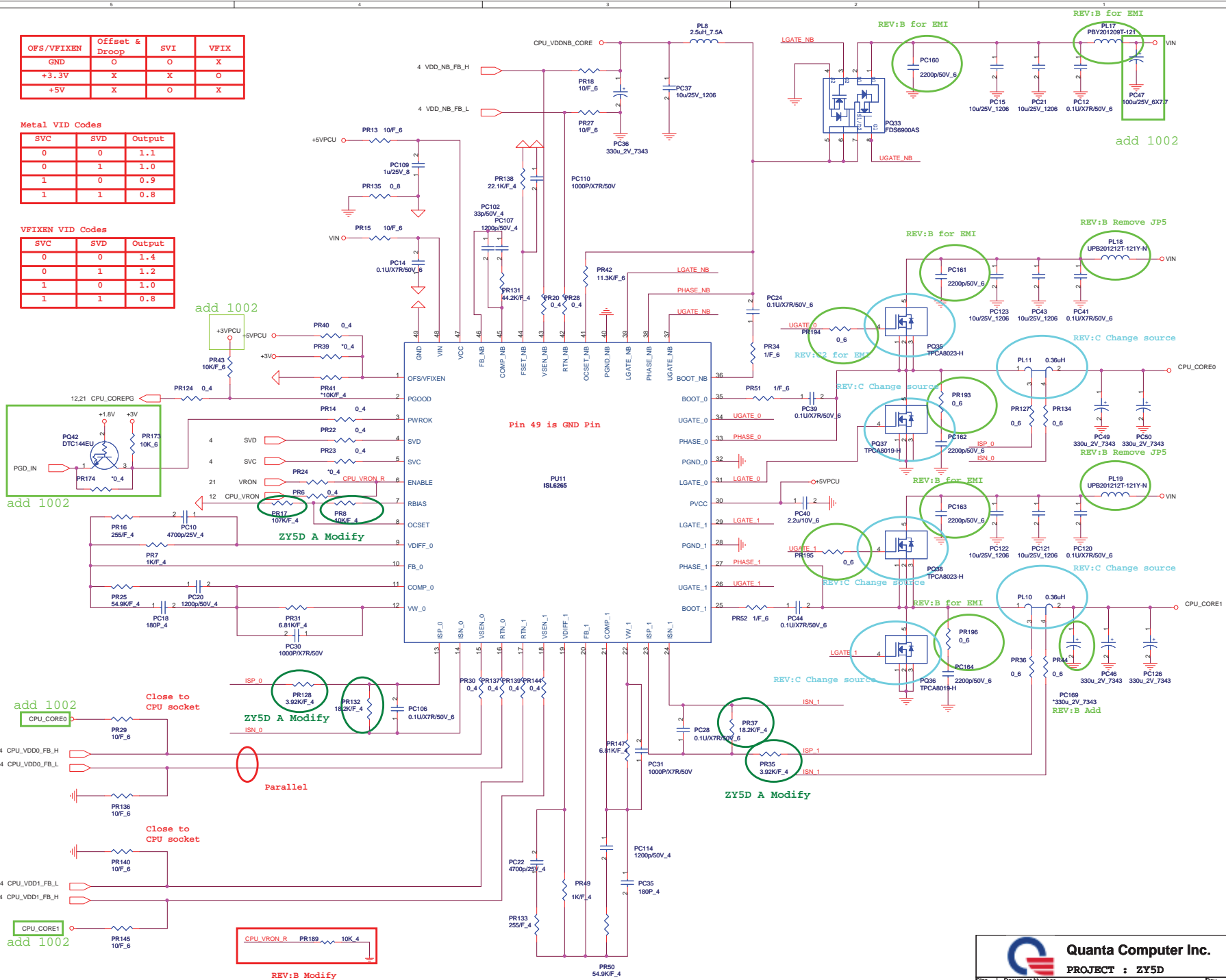
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



add 1002

Pin 49 is GND Pin

ZY5D A Modify

ZY5D A Modify

ZY5D A Modify

Parallel

Close to CPU socket

Close to CPU socket

REV:B Modify

REV:B for EMI

REV:B for EMI

REV:B for EMI

REV:B Remove JP5

REV:B for EMI

REV:C Change source

REV:B for EMI

REV:B Remove JP5

REV:B for EMI

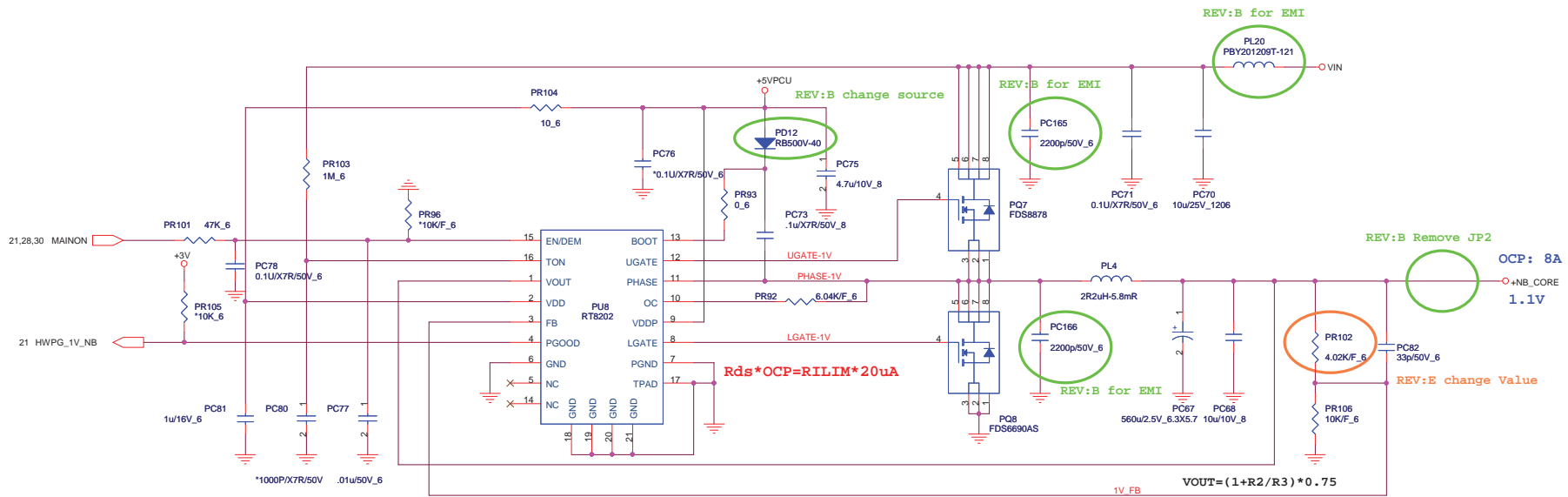
REV:C Change source

REV:B for EMI

REV:B Add

Quanta Computer Inc.
PROJECT : ZY5D

Size: Document Number: **AMD Griffin (ISL6265)** Rev: 38
 Date: Thursday, July 24, 2008 Sheet: 28 of 35

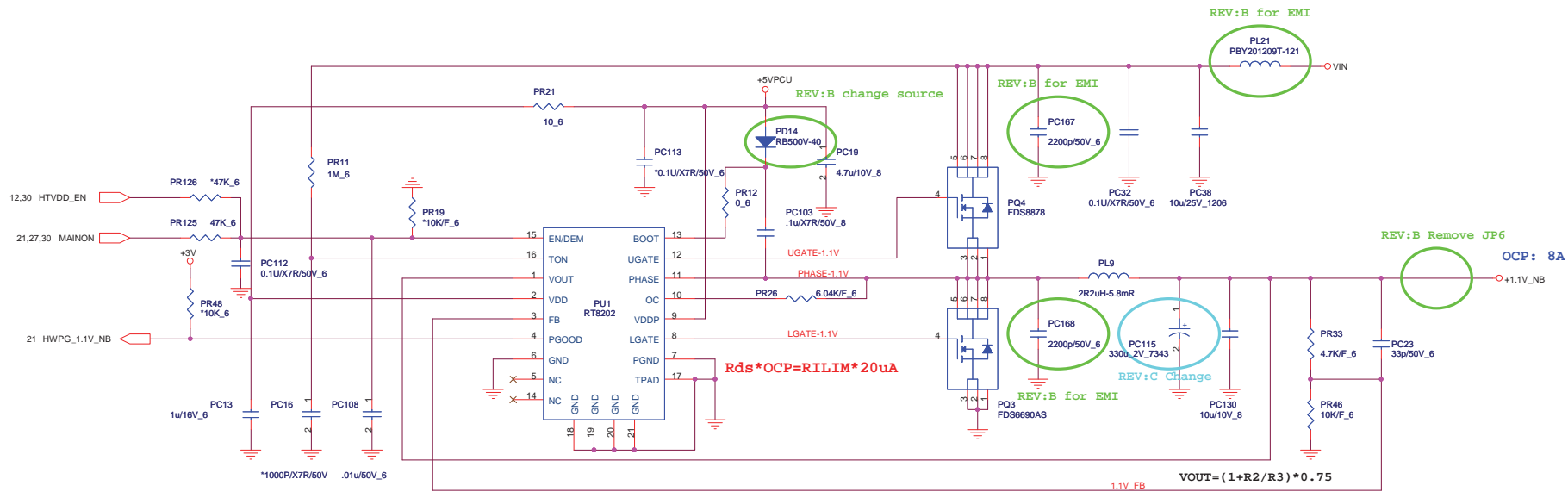


$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$

8A OCP --- OC=6.04K
 FDS6690AS Rds=15mOhm

$Rds * OCP = RILIM * 20uA$

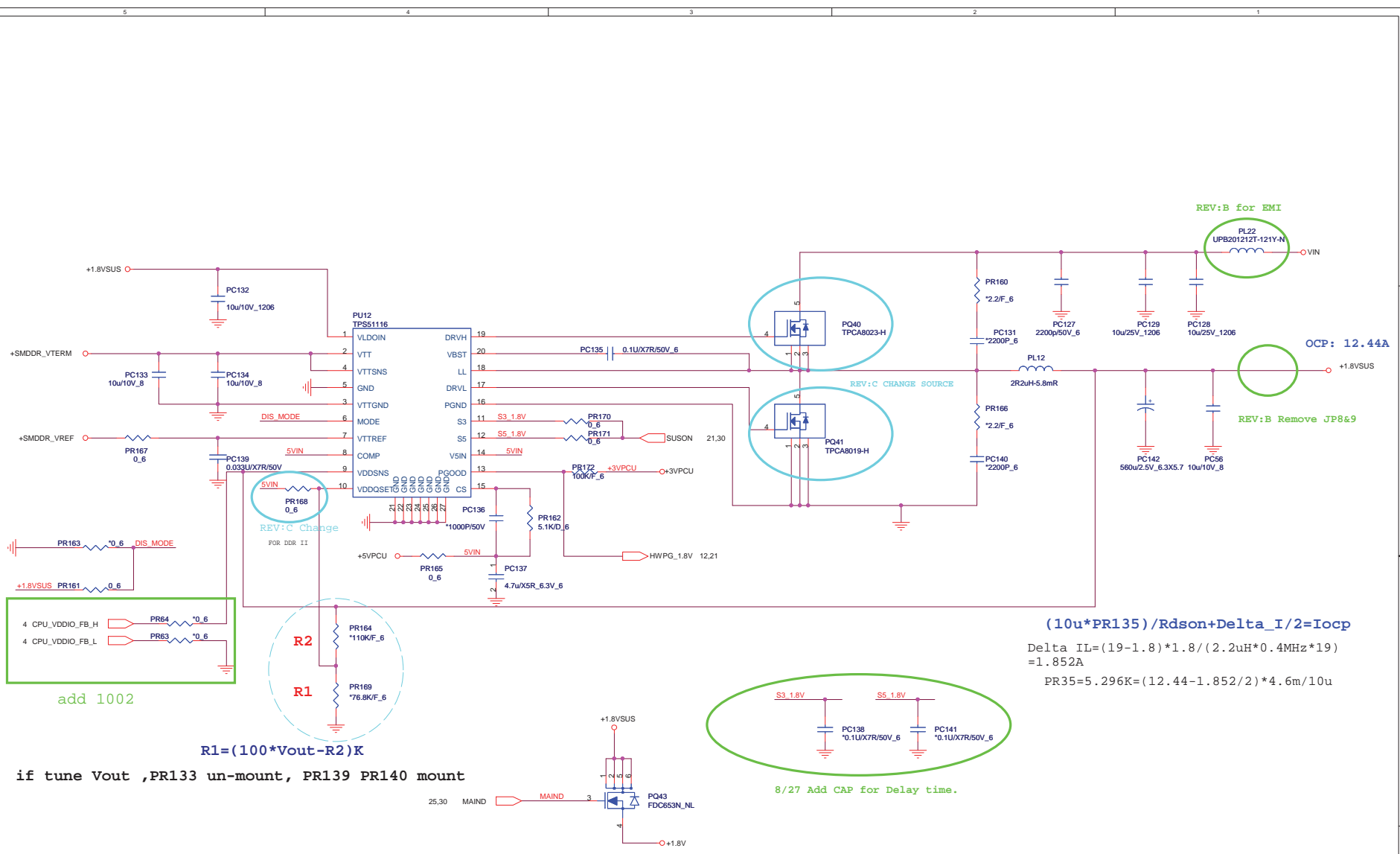
$VOUT = (1 + R2/R3) * 0.75$
 1V_FB



$TON = 3.85p * RTON * Vout / (Vin - 0.5)$
 $Frequency = Vout / (Vin * TON)$

8A OCP --- OC=6.04K
 FDS6690AS Rds=15mOhm

$VOUT = (1 + R2/R3) * 0.75$



$$OCP: 12.44A$$

$$PR35 = \frac{(10u * PR135)}{R_{dson} + \Delta I} = I_{ocp}$$

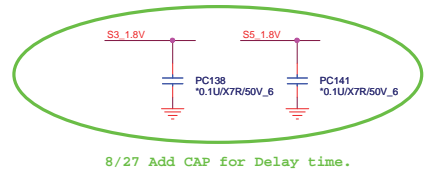
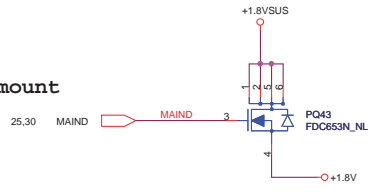
$$\Delta I_L = \frac{(19 - 1.8) * 1.8}{(2.2uH * 0.4MHz * 19)} = 1.852A$$

$$PR35 = 5.296K = (12.44 - 1.852 / 2) * 4.6m / 10u$$

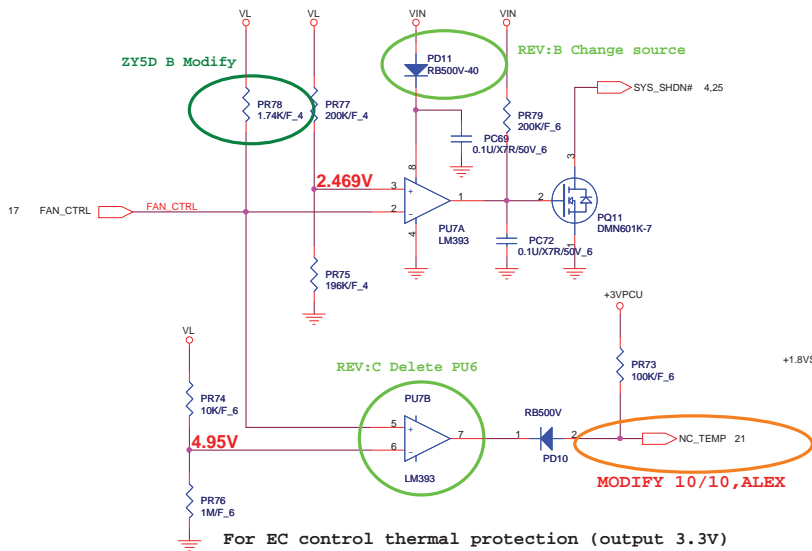
add 1002

$$R1 = (100 * V_{out} - R2)K$$

if tune Vout ,PR133 un-mount, PR139 PR140 mount

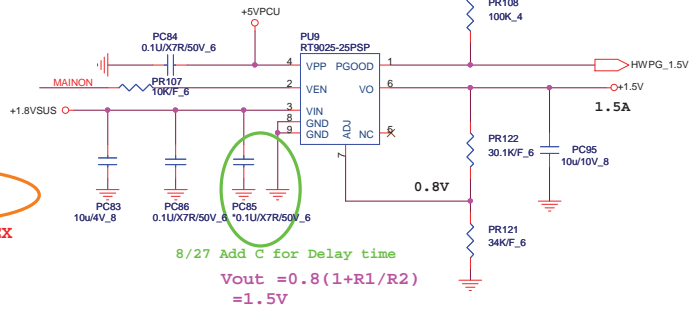


NTC resistor on Thermal module

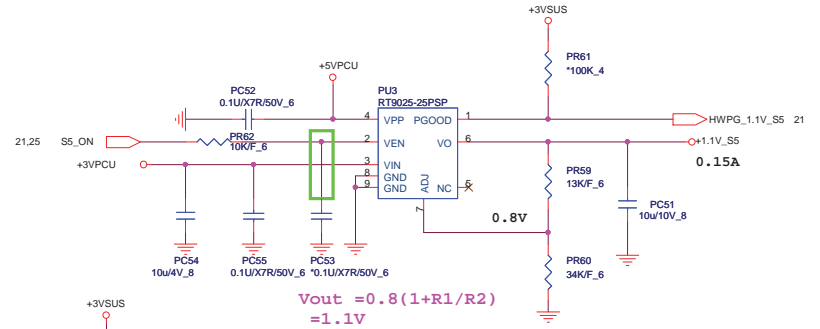


For EC control thermal protection (output 3.3V)

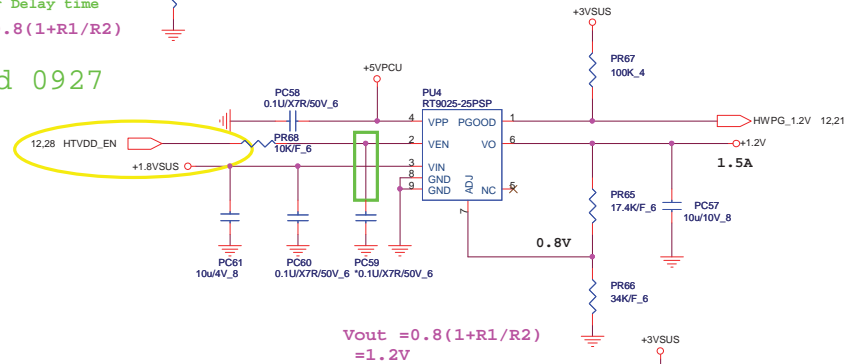
add 0927



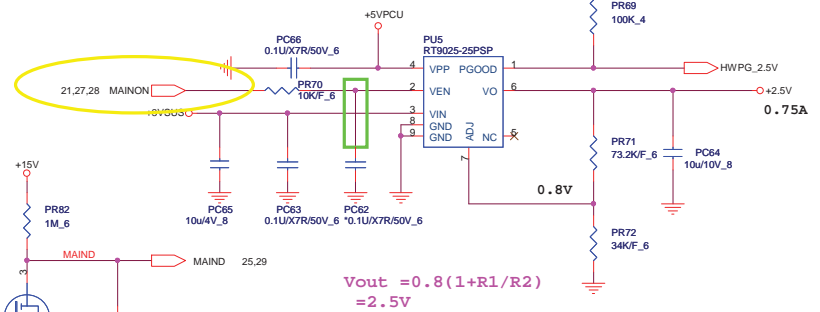
add 0927



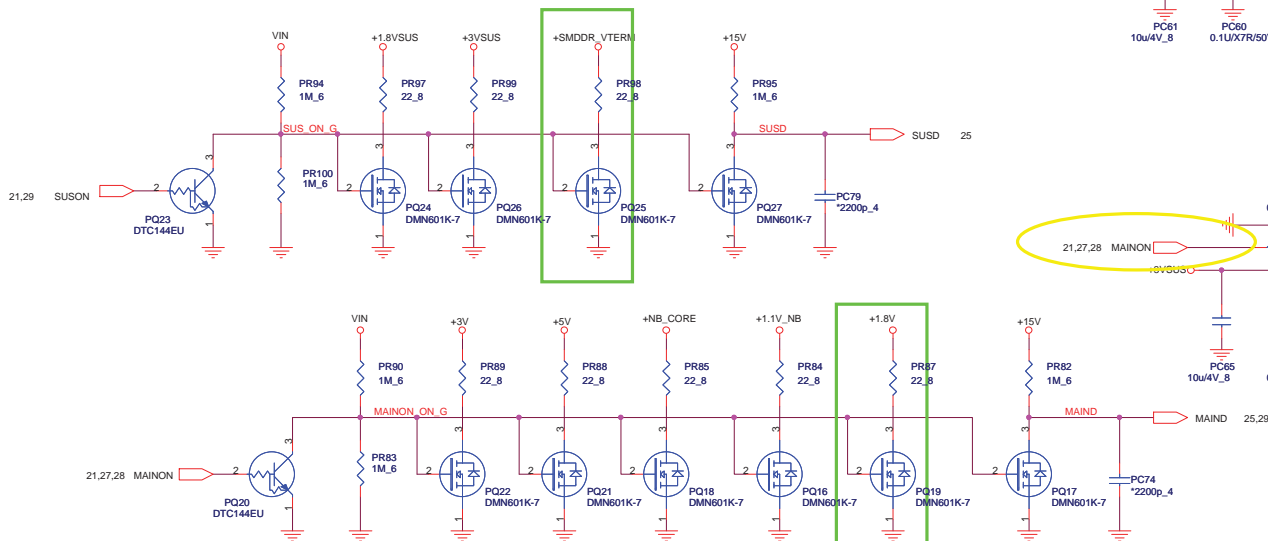
add 0927




Vout = 0.8(1+R1/R2) = 1.2V

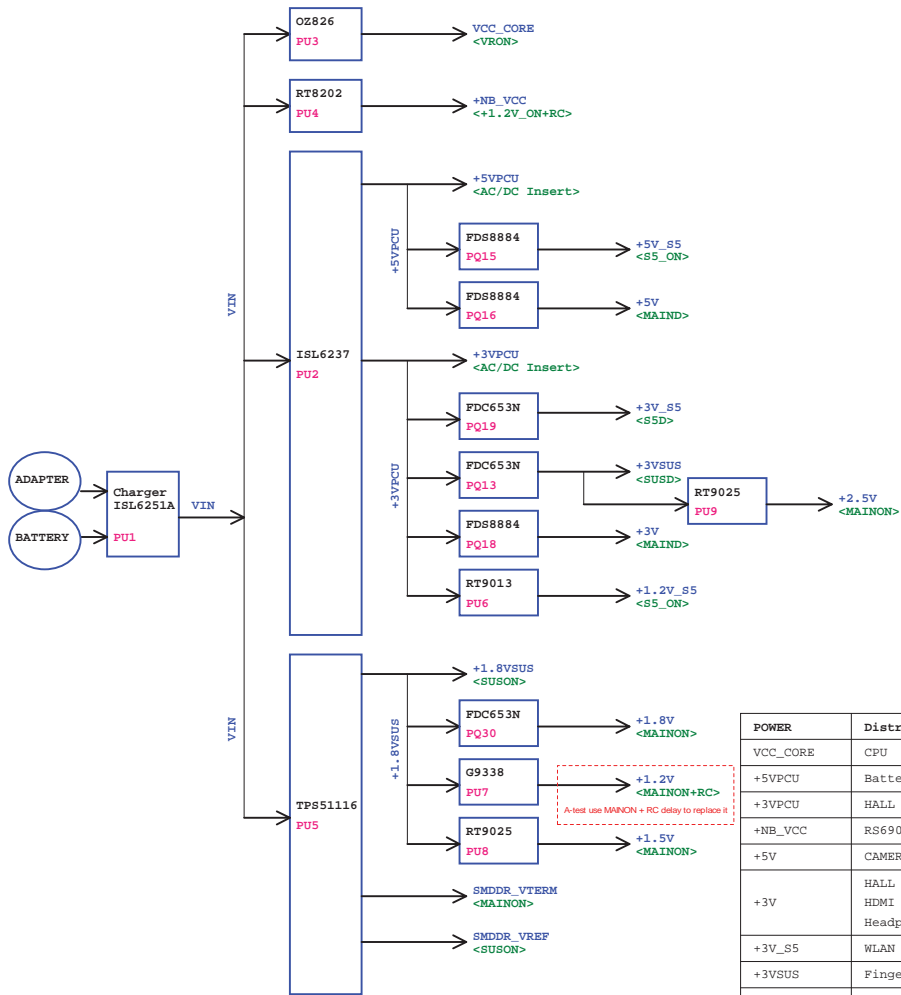


Vout = 0.8(1+R1/R2) = 2.5V



add 1002

 Quanta Computer Inc. PROJECT : ZY5D		Rev
		3B
Size	Document Number	
Discharge (1.1V/1.2V/2.5V)		
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POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_VCC	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VVSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	

ZY5 Power on Sequence

