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**Samsung**  
**NP-N100S, NP-N102S**

**Eric-VE-R**

**ENE micom**

CPU : INTEL CEDARVIEW-M  
 Chip Set : INTEL TIGERPOINT-M  
 Remarks : DC, DDR3

Model Name : Eric-VE-R  
 PCB Part No : BA41-01868A(GCE)  
 BA41-01869A(GBM)  
 BA41-01871A(PIOTEC)

Dev. Step : PR  
 Revision : 1.0  
 T.R. Date : 2011.12.12

DRAW	CHECK	APPROVAL
Qin Wenchao	Wu shijiang	BC LEE

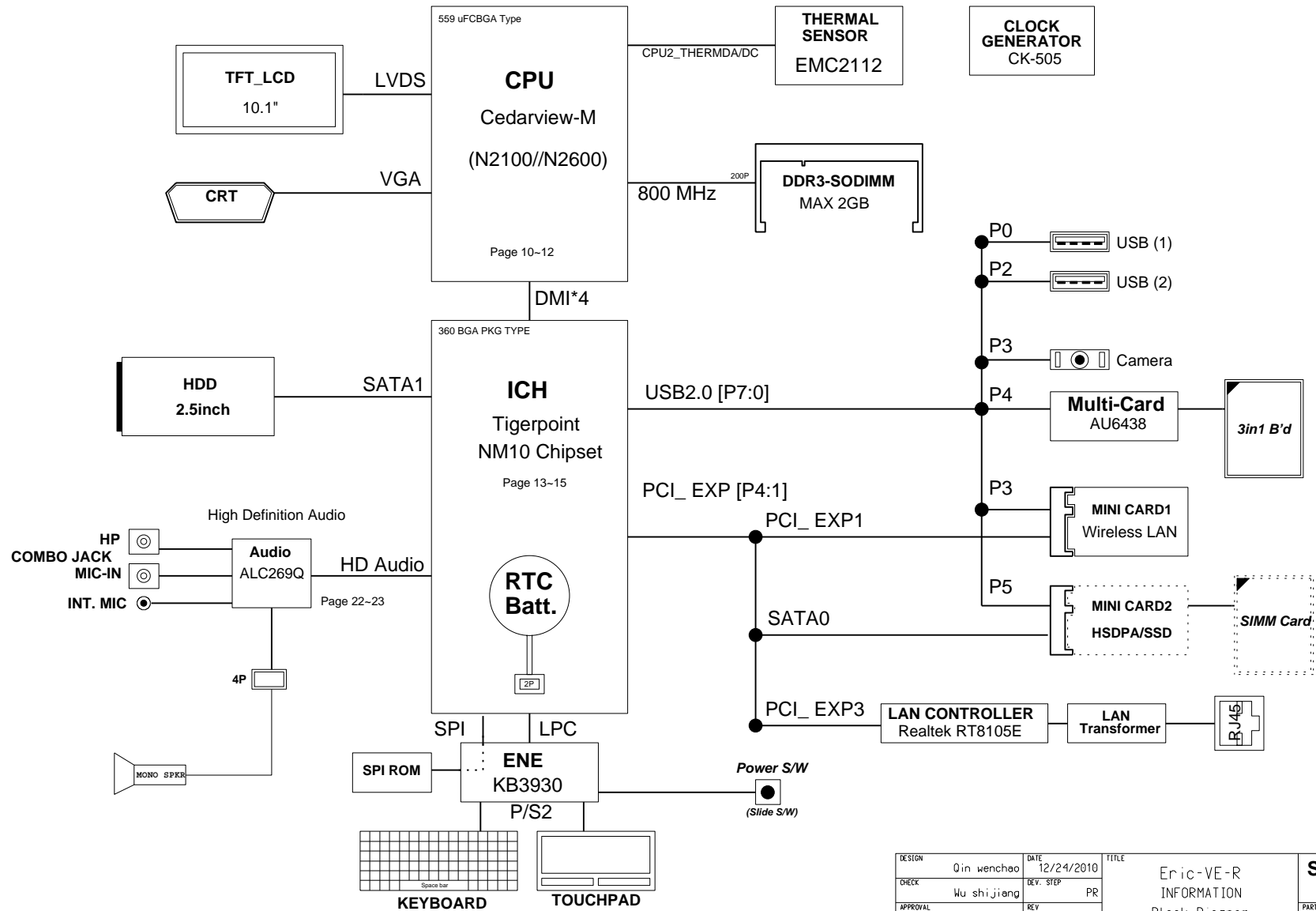
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DESIGN	Qin wenchao	DATE	11/25/2011	TITLE	Eric-VE-R MAIN COVER	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	PR	PART NO.			BA41-0XXXXA
APPROVAL	BC LEE	REV	1.0				
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE			1 OF 42

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# OPERATION BLOCK DIAGRAM



DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R INFORMATION Block Diagram	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM			
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# BOARD INFORMATION

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### Power Sequence Timing



### PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB Hub to PCI	AD29(internal)		
LPC Bridge/IDE/AC97/SMBUS	AD30(internal)		
Internal MAC	AD31(internal)		
	AD24(internal)	Programmable	

### I<sup>2</sup>C / SMB Address

Devices	Address	Hex	Bus
TigerPoint	Master		SMBUS Master
OK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMMO	1010 000X	A0h	
CPU Thermal Sensor	0111 101X	7Ah	Thermal Sensor

### USB PORT Assign

Port Number	ASSIGNED TO	Port Number	ASSIGNED TO
UHCL_0	0 USB Port_P0	UHCL_2	4 MMC
	1 NC	UHCL_3	5 Mini Card 2(For HSDPA)
UHCL_1	2 USB Port_P2		6 NC
	3 Mini Card 1(For WLAN)		7 CAMERA

### PCI Express Assign

Port Number	ASSIGNED TO
1	Mini Card 1(Wireless LAN)
2	NC
3	LOM
4	NC

### Voltage Rails

Power Rail	Descriptions
PRTC_BAT	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well.
VDC	Primary DC system power supply (9 to 19V)
P1.05V(VCCP)	VTT for CPU, Calistoga & ICH7-M
P3.3V_MICOP	3.3V always power rail(for Microm)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail for DDR (off in S4-S5)
P0.75V	0.75V power rail for DDR (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
CPU_CORE	Core voltage for Atom CPU
P1.8V	For display logic of CPU

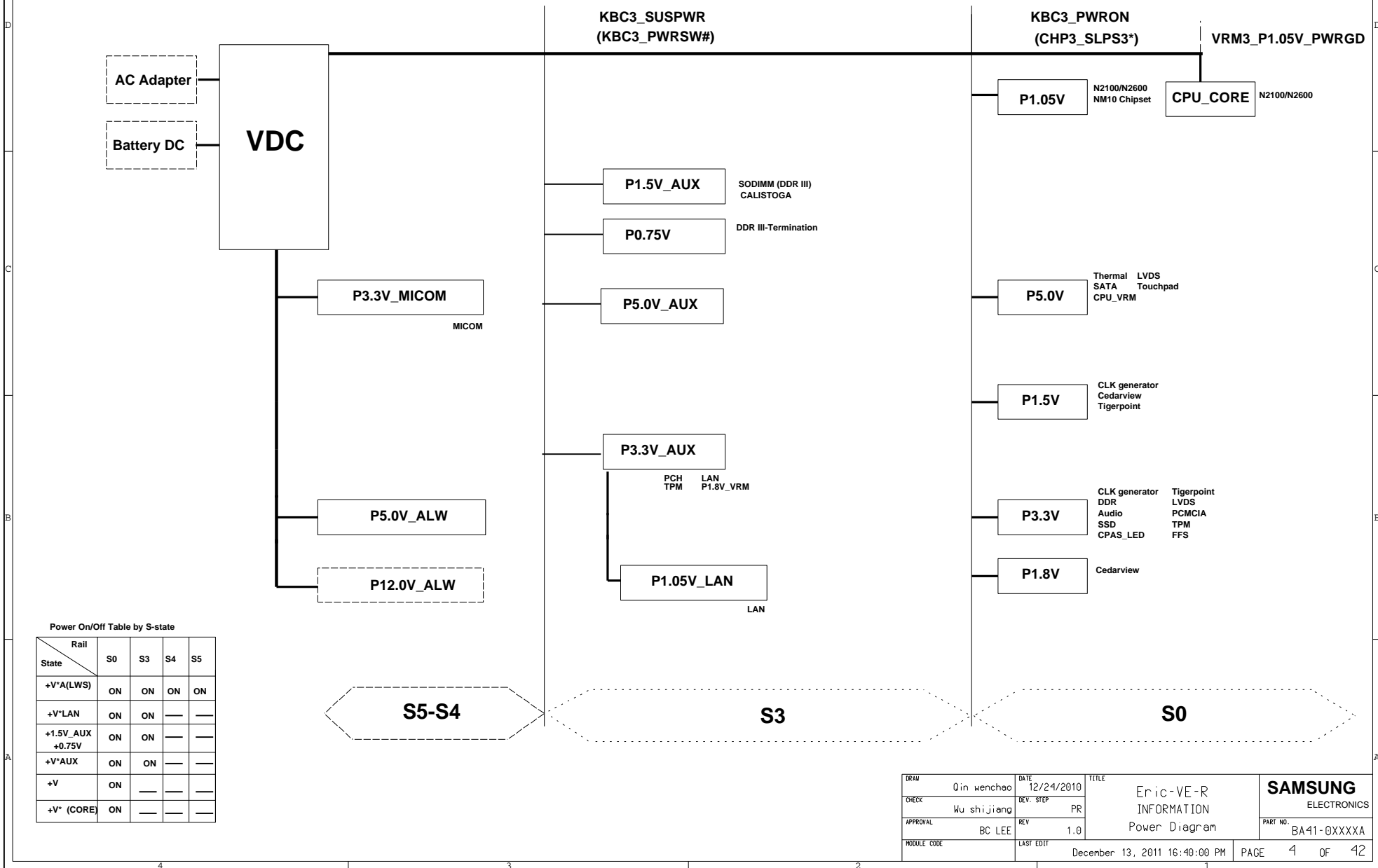
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CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	3	OF 42

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# POWER DIAGRAM

Rev 1.0



Power On/Off Table by S-state

Rail \ State	S0	S3	S4	S5
+V*A(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	---	---
+1.5V_AUX +0.75V	ON	ON	---	---
+V*AUX	ON	ON	---	---
+V	ON	---	---	---
+V* (CORE)	ON	---	---	---

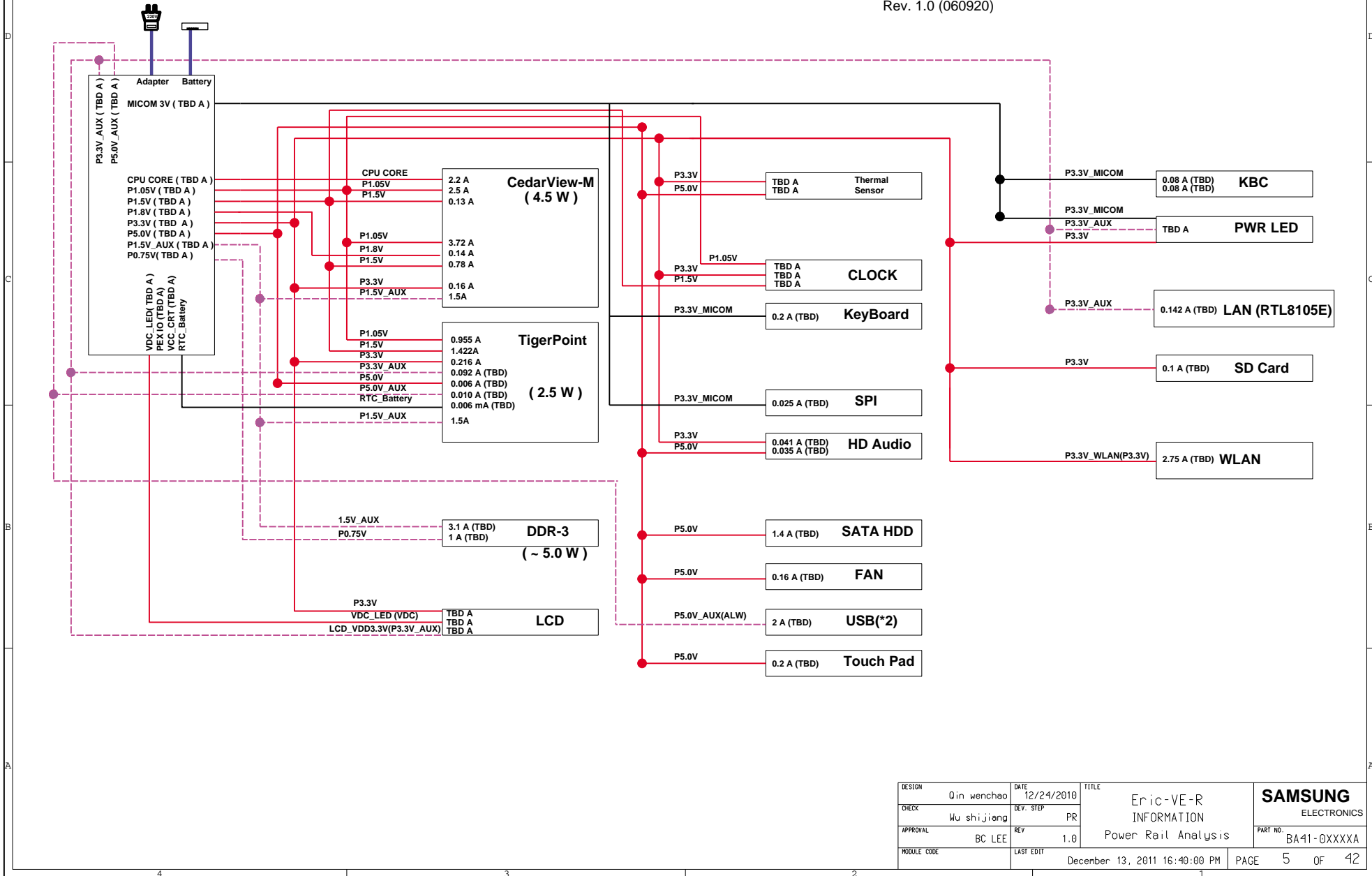
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CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE 4 OF 42		

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# POWER RAILS ANALYSIS

Rev. 1.0 (060920)

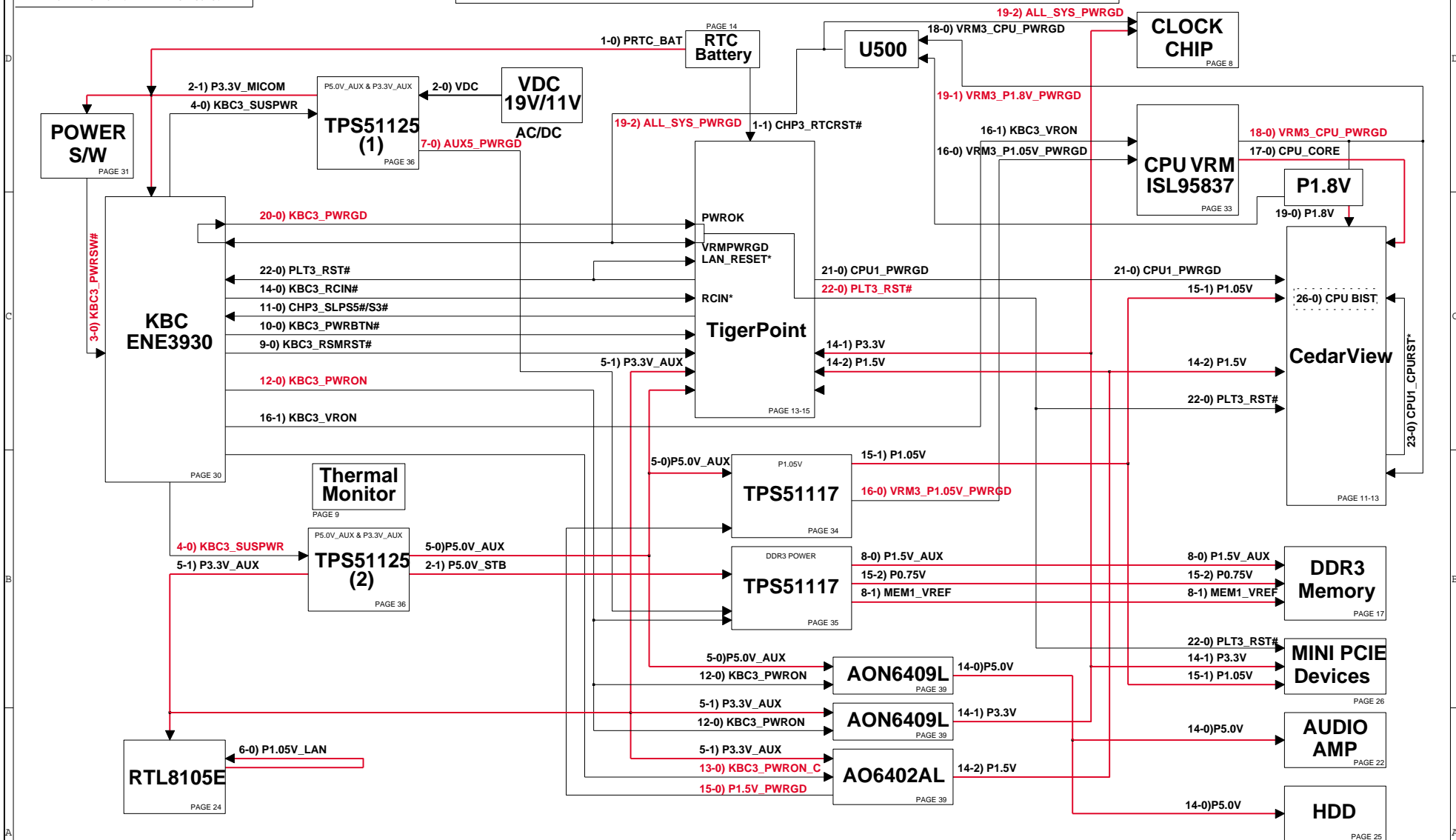


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CHECK	Wu shijiang	DEV. STEP	PR	Power Rail Analysis		
APPROVAL	BC LEE	REV	1.0	December 13, 2011 16:40:00 PM		PAGE 5 OF 42
MODULE CODE		LAST EDIT				

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# POWER SEQUENCE BLOCK DIAGRAM



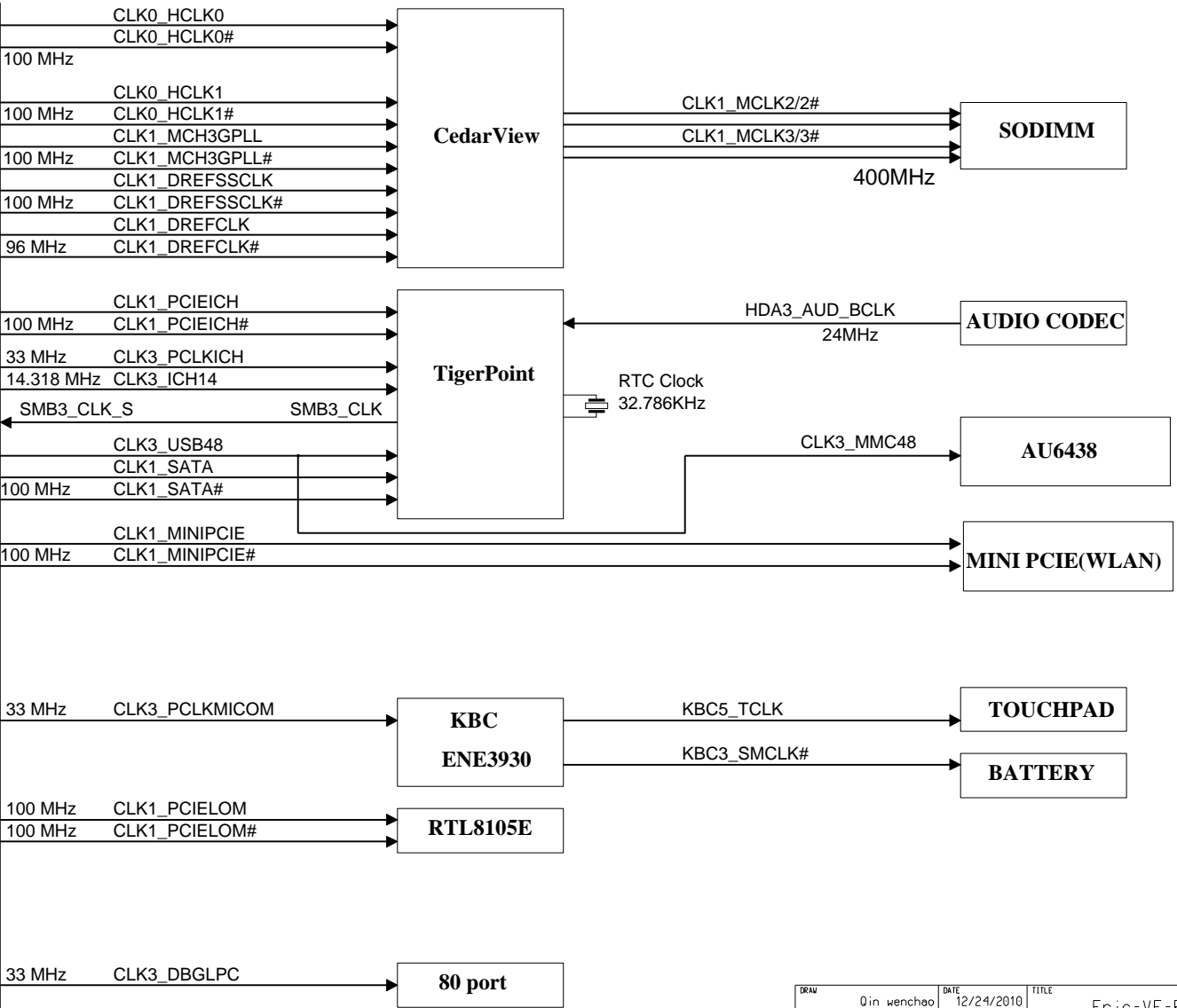
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APPROVAL	BC LEE	REV	1.0	Power Sequence Block		PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	6	OF 42

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# CLOCK DISTRIBUTION

1205-002574  
**CLOCK GENERATOR**  
**CK-505M**  
**SLG8LV631V**

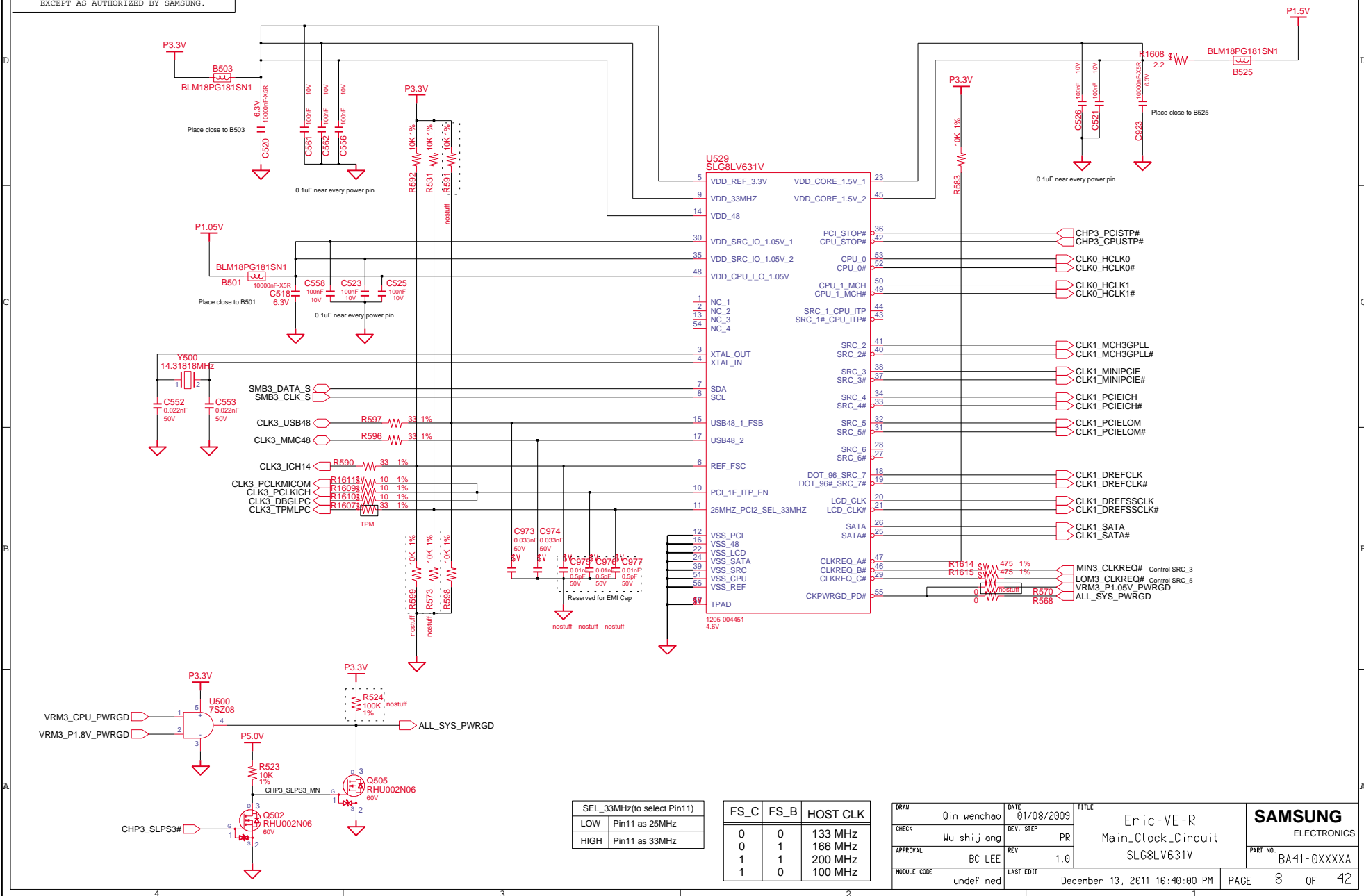


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CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE 7 OF 42		

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# CLOCK GENERATOR



SEL_33MHz(to select Pin11)	
LOW	Pin11 as 25MHz
HIGH	Pin11 as 33MHz

FS_C	FS_B	HOST CLK
0	0	133 MHz
0	1	166 MHz
1	1	200 MHz
1	0	100 MHz

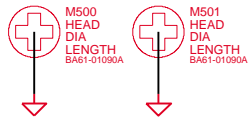
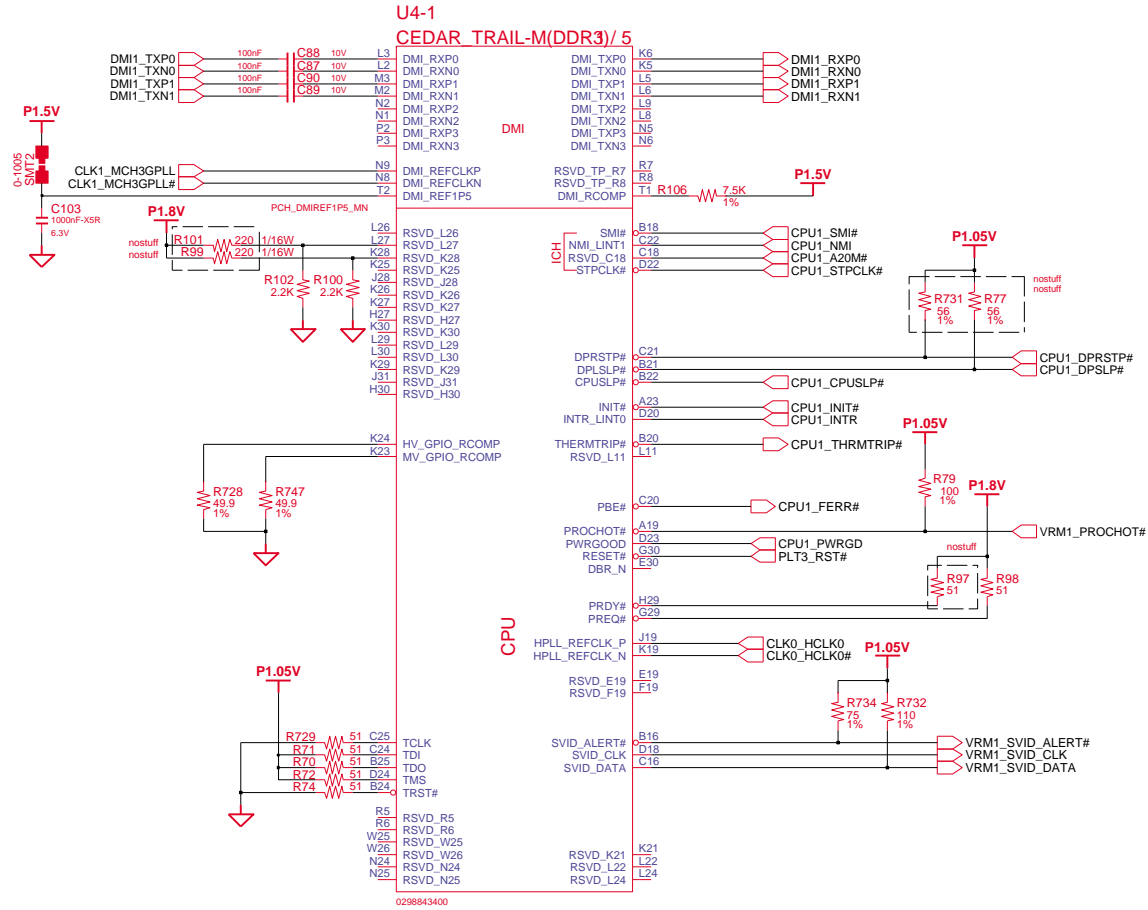
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MODULE CODE	undefined	LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	8	OF 42





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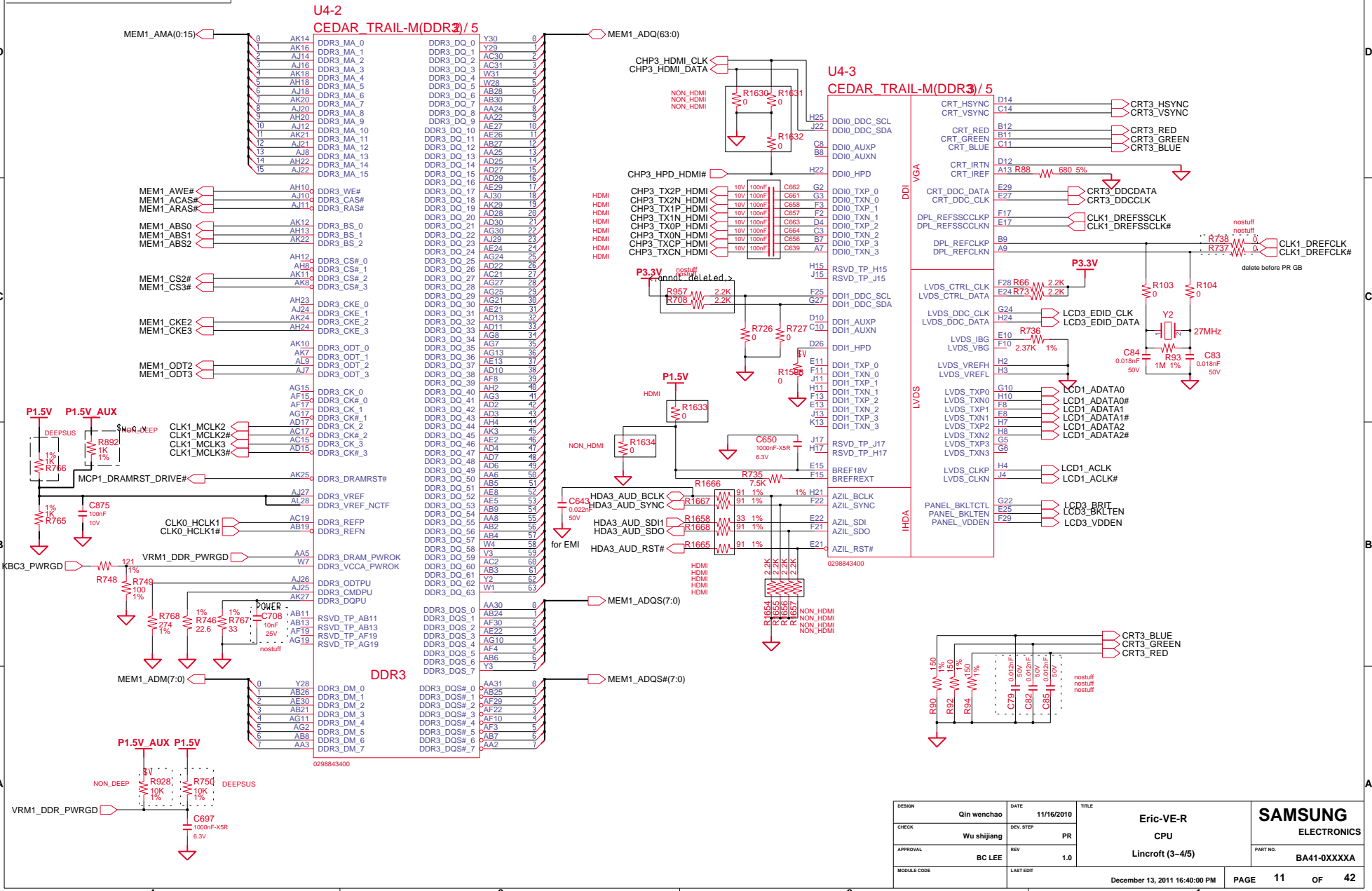
## CEDAR TRAIL PROCESSOR (1/3)



DRAW	Qin wenchao	DATE	11/16/2010	TITLE	Eric-VE-R	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	PR		CPU		
APPROVAL	BC LEE	REV	1.0		Lincroft (2/5)	PART NO. BA41-0XXXXA	
MODULE CODE		LAST EDIT					
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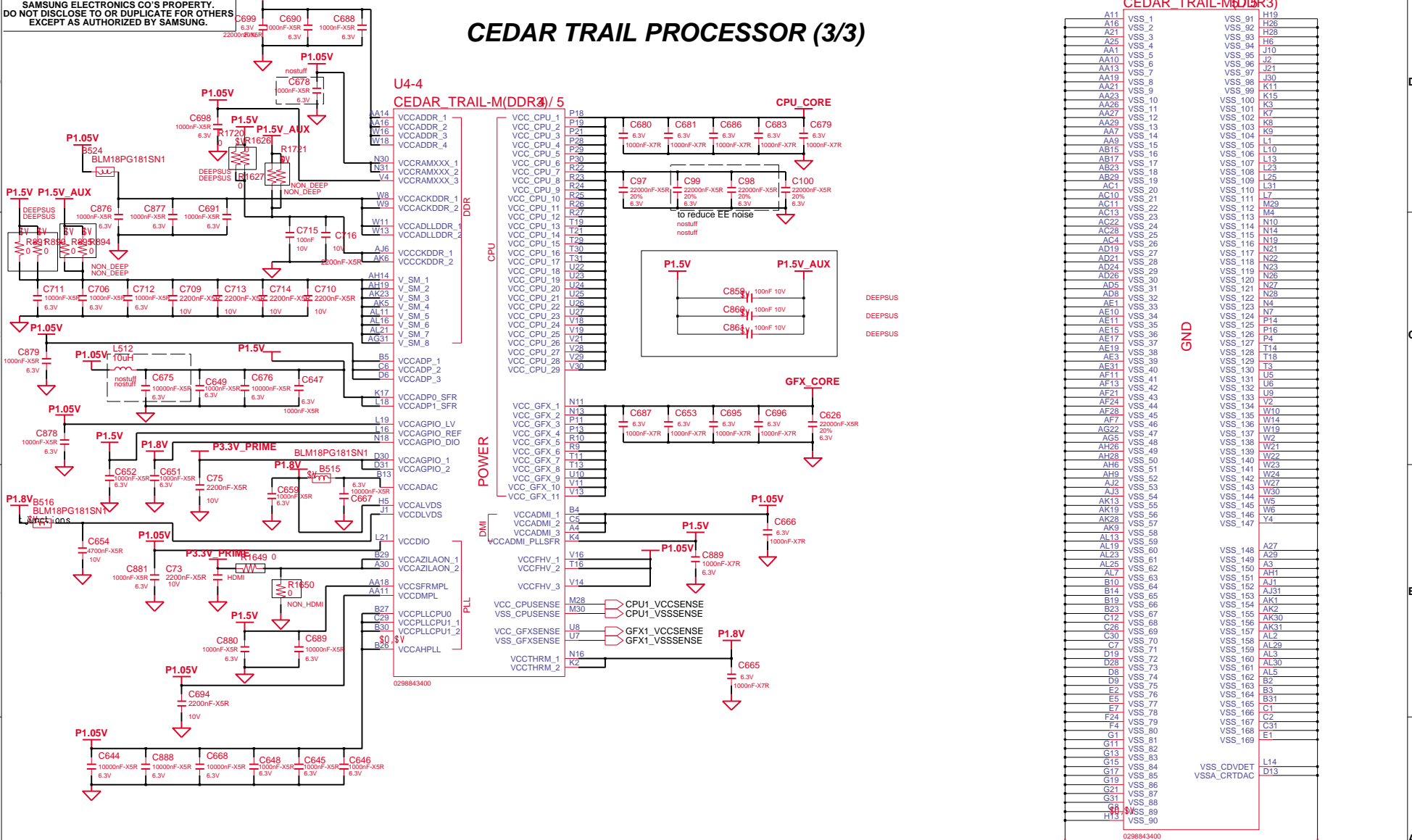
# CEDAR TRAIL PROCESSOR (2/3)



DESIGN	Qin wenchao	DATE	11/16/2010	TITLE	Eric-VE-R	SAMSUNG ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	PR		CPU		PART NO. BA41-0XXXXA
APPROVAL	BC LEE	REV	1.0		Lincroft (3-4/5)		
MODULE CODE		LAST EDIT					
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# CEDAR TRAIL PROCESSOR (3/3)



## U4-5 CEDAR TRAIL-M(DDR3)

A11	VSS_1	H19
A16	VSS_2	H26
A21	VSS_3	H28
A25	VSS_4	H6
AA1	VSS_5	J10
AA10	VSS_6	J2
AA13	VSS_7	J21
AA19	VSS_8	J30
AA21	VSS_9	K11
AA23	VSS_10	K15
AA26	VSS_11	K3
AA27	VSS_12	K7
AA29	VSS_13	K8
AA7	VSS_14	K9
AA9	VSS_15	L1
AB15	VSS_16	L13
AB17	VSS_17	L23
AB23	VSS_18	L25
AB29	VSS_19	L31
AC1	VSS_20	L7
AC10	VSS_21	M29
AC11	VSS_22	M4
AC13	VSS_23	M4
AC22	VSS_24	N10
AC28	VSS_25	N14
AC4	VSS_26	N19
AD19	VSS_27	N21
AD21	VSS_28	N22
AD24	VSS_29	N23
AD26	VSS_30	N28
AD5	VSS_31	N27
AD8	VSS_32	N28
AE1	VSS_33	N4
AE10	VSS_34	N7
AE11	VSS_35	P14
AE15	VSS_36	P16
AE17	VSS_37	P4
AE19	VSS_38	T14
AE3	VSS_39	T3
AE31	VSS_40	T3
AF11	VSS_41	U5
AF13	VSS_42	U6
AF21	VSS_43	U9
AF24	VSS_44	Y2
AF28	VSS_45	W10
AF7	VSS_46	W14
AG22	VSS_47	W19
AG5	VSS_48	W2
AH26	VSS_49	W21
AH28	VSS_50	W22
AH6	VSS_51	W23
AH9	VSS_52	W24
AJ2	VSS_53	W27
AJ3	VSS_54	W30
VSS_55	VSS_55	W5
AK13	VSS_56	W6
AK19	VSS_57	W6
AK28	VSS_58	Y4
AK9	VSS_59	
AL13	VSS_60	A27
AL19	VSS_61	A29
AL23	VSS_62	A3
AL26	VSS_63	AH1
AL7	VSS_64	AH1
B10	VSS_65	AJ1
B14	VSS_66	AJ3
B19	VSS_67	AK1
B23	VSS_68	AK2
C12	VSS_69	AK30
C26	VSS_70	AK31
C30	VSS_71	AK32
C7	VSS_72	AL29
D19	VSS_73	AL5
D28	VSS_74	AL30
D8	VSS_75	AL5
D9	VSS_76	B2
E2	VSS_77	B3
E5	VSS_78	B1
E7	VSS_79	C1
F4	VSS_80	C2
G1	VSS_81	C31
G11	VSS_82	E1
G13	VSS_83	
G15	VSS_84	L14
G17	VSS_85	D13
G19	VSS_86	
G21	VSS_87	
G31	VSS_88	
H8	VSS_89	
H19	VSS_90	

DESIGN	Qin wenchao	DATE	11/16/2010	TITLE	Eric-VE-R	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR		CPU	
APPROVAL	BC LEE	REV	1.0		Lincroft (5/5)	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT			December 13, 2011 16:40:00 PM	PAGE 12 OF 42

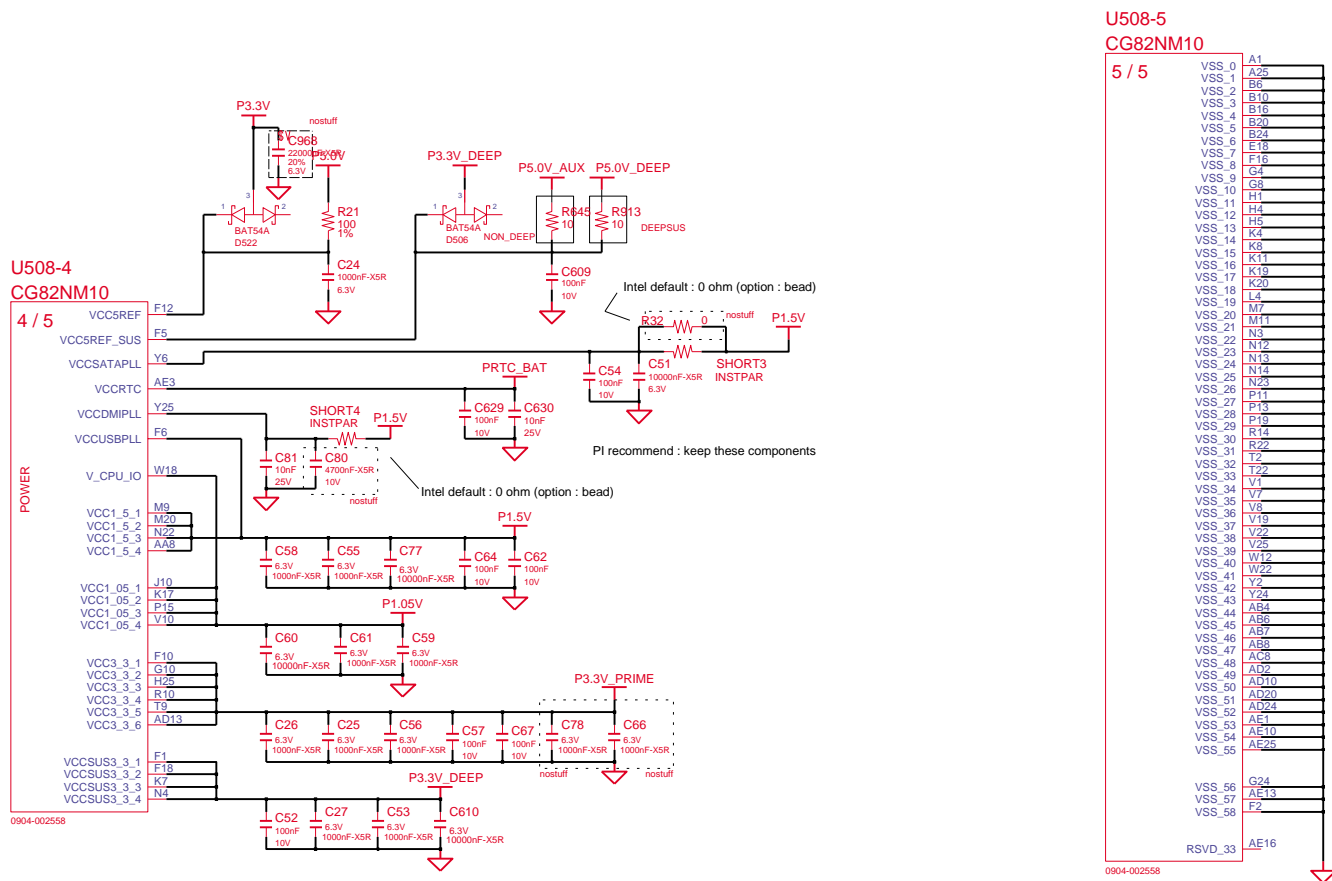




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# Tigerpoint (3/3)



U508-5

CG82NM10

5 / 5

VSS_0	A1
VSS_1	A25
VSS_2	B6
VSS_3	B10
VSS_4	B18
VSS_5	B20
VSS_6	B24
VSS_7	E18
VSS_8	F16
VSS_9	G4
VSS_10	G8
VSS_11	H1
VSS_12	H4
VSS_13	H5
VSS_14	K4
VSS_15	K8
VSS_16	K11
VSS_17	K18
VSS_18	K20
VSS_19	L4
VSS_20	M7
VSS_21	M11
VSS_22	N3
VSS_23	N12
VSS_24	N13
VSS_25	N14
VSS_26	N23
VSS_27	P11
VSS_28	P13
VSS_29	P19
VSS_30	R14
VSS_31	R22
VSS_32	T2
VSS_33	T22
VSS_34	V1
VSS_35	V7
VSS_36	V8
VSS_37	V19
VSS_38	V22
VSS_39	V25
VSS_40	W12
VSS_41	W22
VSS_42	Y2
VSS_43	Y24
VSS_44	AB4
VSS_45	AB7
VSS_46	AB8
VSS_47	AC3
VSS_48	AD2
VSS_49	AD10
VSS_50	AD20
VSS_51	AD24
VSS_52	AE1
VSS_53	AE10
VSS_54	AE13
VSS_55	AE25
VSS_56	G24
VSS_57	AE13
VSS_58	F2
RSVD_33	AE16

0904-002558

DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R CHIPSET TIGERPOINT(3/3)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
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# 80H DECODER CONNECTOR AND DEBUG CODE

## AMI Aptio 4.x Status Codes

### ACPI/ASL Status Codes

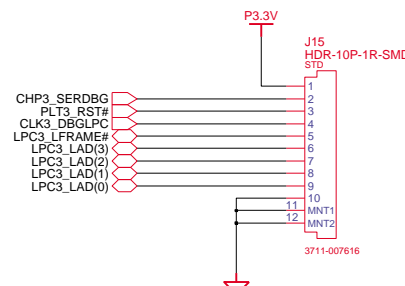
- 01 System is entering S1 sleep state
- 02 System is entering S2 sleep state
- 03 System is entering S3 sleep state
- 04 System is entering S4 sleep state
- 05 System is entering S5 sleep state
- 10 System is waking up from the S1 sleep state
- 20 System is waking up from the S1 sleep state
- 30 System is waking up from the S1 sleep state
- 40 System is waking up from the S1 sleep state
- AC System has transitioned into ACPI mode(PCI)
- AA System has transitioned into ACPI mode(ACPI)

### PEI Status Codes

- Progress Codes**
- 10 PEI Core is started
  - 11 Pre-memory CPU initialization is started
  - 12 Pre-memory CPU initialization(CPU module specific)
  - 13 Pre-memory CPU initialization(CPU module specific)
  - 14 Pre-memory CPU initialization(CPU module specific)
  - 15 Pre-memory North Bridge initialization is started
  - 16 Pre-memory North Bridge initialization(North Bridge module specific)
  - 17 Pre-memory North Bridge initialization(North Bridge module specific)
  - 18 Pre-memory Bridge initialization(North Bridge module specific)
  - 19 Pre-memory South Bridge initialization is started
  - 1A Pre-memory South Bridge initialization (South Bridge module specific)
  - 1B Pre-memory South Bridge initialization (South Bridge module specific)
  - 1C Pre-memory South Bridge initialization (South Bridge module specific)
  - 1D-2A OEM pre -memory initialization codes
  - 2B Memory initialization.Serial Presence Detect (SPD) data reading
  - 2C Memory initialization.MemoryI presence Detection
  - 2D Memory initialization. Programming memory timing information
  - 2E Memory initialization. Configuring memory
  - 2F Memory initialization.(other)
  - 30 Reserved for ASL (see ASL Statue Codes section below)
  - 31 Memory installed
  - 32 CPU post-memory initialization is started
  - 33 CPU post-memory initialization. Cache initialization
  - 34 CPU post-memory initialization. Application Processor(s) (AP) initialization
  - 35 CPU post-memory initialization. Boot Strap Processor(BSP) selection
  - 36 CPU post-memory initialization. System Management Mode (SMM) initialization
  - 37 Post-Memory North Bridge initialization is started
  - 38 Post-Memory North Bridge initialization (North Bridge module specific)
  - 39 Post-Memory North Bridge initialization (North Bridge module specific)
  - 3A Post-Memory North Bridge initialization (North Bridge module specific)
  - 3B Post-Memory South Bridge initialization is started
  - 3C Post-Memory South Bridge initialization (South Bridge module specific)
  - 3D Post-Memory South Bridge initialization (South Bridge module specific)
  - 3E Post-Memory South Bridge initialization (South Bridge module specific)
  - 3F-4E OEM post memory initialization codes
  - 4F DXE IPL is started
- PEI Error Codes**
- 50 Memory initialization error.Invalid memory type or incompatible memory speed.
  - 51 Memory initialization error.SPD reading has failed
  - 52 Memory initialization error.Invalid memory size or memory modules do not match
  - 53 Memory initialization error.No useable memory detected
  - 54 Unspecified memory initialization error
  - 55 Memory not installed
  - 56 Invalid CPU type or Speed
  - 57 CPU mismatch
  - 58 CPU self test failed or possible CPU cache error
  - 59 CPU micro-code is not found or micro-code update is failed
  - 5A Internal CPU error
  - 5B reset PPI is not available
  - 5C-5F Reserved for future AMI error codes
- S3 Resume Progress Codes**
- E8 S3 Resume Failed in PEI
  - E9 S3 Resume PPI not Found
  - FA S3 Resume Boot Script Error
  - FB S3 OS Wake Error
  - FC-EF Reserved for future AMI error codes
- Recovery Progress Codes**
- F0 Recovery condition triggered by firmware(Auto recovery)
  - F1 Recovery condition triggered by user(Forced recovery)
  - F2 Recovery process started
  - F3 Recovery firmware image is found
  - F4 Recovery firmware image is loaded
  - F5-F7 Reserved for future AMI progress codes
- Recovery Error Codes**
- F8 Recovery PPI is not available
  - F9 Recovery capsule is not found
  - FA Invalid recovery capsule
  - FB-FF Reserved for future AMI error codes
  - 5A Internal CPU error
  - 5B reset PPI is not available
  - 5C-5F Reserved for future AMI error codes

### DXE Status Codes

- Progress Codes**
- 60 DXE Core is started
  - 61 NVRAM initialization
  - 62 Installation to the South Bridge Runtime Services
  - 63 CPU DXE initialization is started
  - 64 CPU DXE initialization(CPU module specific)
  - 65 CPU DXE initialization(CPU module specific)
  - 66 CPU DXE initialization(CPU module specific)
  - 67 CPU DXE initialization(CPU module specific)
  - 68 PCI host bridge initialization
  - 69 North Bridge DXE initialization is started
  - 6A North Bridge DXE SMM initialization is started
  - 6B North Bridge DXE initialization(North Bridge module specific)
  - 6C North Bridge DXE initialization(North Bridge module specific)
  - 6D North Bridge DXE initialization(North Bridge module specific)
  - 6E North Bridge DXE initialization(North Bridge module specific)
  - 6F North Bridge DXE initialization(North Bridge module specific)
  - 70 South Bridge DXE initialization is started
  - 71 South Bridge DXE SMM initialization is started
  - 72 South Bridge devices initialization
  - 73 South Bridge DXE SMM initialization(South Bridge module specific)
  - 74 South Bridge DXE initialization(South Bridge module specific)
  - 75 South Bridge DXE initialization(South Bridge module specific)
  - 76 South Bridge DXE initialization(South Bridge module specific)
  - 77 South Bridge DXE initialization(South Bridge module specific)
  - 78 ACPI module initialization
  - 79 CSM initialization
  - 7A-7F Reserved for future AMI DEX codes
  - 80-8F OEM DEX initialization codes
  - 90 Boot Device Selection (BDS) phase is started
  - 91 Driver connecting is started
  - 92 PCI Bus initialization is started
  - 93 PCI Bus Hot Plug Controller Initialization
  - 94 PCI Bus Enumeration
  - 95 Bus Request Resources
  - 96 PCI Bus Assign Resources
  - 97 Console Output devices connect
  - 98 Console Input devices connect
  - 99 Super IO Initialization
  - 9A USB initialization is started
  - 9B USB Reset
  - 9C USB Detect
  - 9D USB Enable
  - 9E-9F Reserved for future AMI codes
  - AC IDE initialization is started
  - A1 IDE Reset
  - A2 IDE Detect
  - A3 IDE Enable
  - A4 SCSI initialization is started
  - A5 SCSI Reset
  - A6 SCSI Detect
  - A7 SCSI Enable
  - A8 Setup Verifying Password
  - A9 Start of Setup
  - AA Reserved for ASL (see ASL Status Codes section below)
  - AB Setup Input Wait
  - AC Reserved for ASL (see ASL Status Codes section below)
  - AD Ready to Boot event
  - AE Legacy Boot Event
  - AF Exit Boot Services event
  - B0 Runtime Set Virtual Address MAP Begin
  - B1 Runtime Set Virtual MAP End
  - B2 Legacy Option ROM Initialization
  - B3 System Reset
  - B4 USB Hot Plug
  - B5 PCI Bus Hot Plug
  - B6 Clean-up of NVRAM
  - B7 Configuration Reset (reset of NVRAM settings)
  - B8-BF Reserved for future AMI codes
  - CO-CF OEM BDS initialization codes
- DXE Error Codes**
- D0 CPU initialization error
  - D1 North Bridge initialization error
  - D2 South Bridge initialization error
  - D3 Some of the Architectural Protocols are not available
  - D4 PCI resource allocation error.Out of Resources
  - D5 No Space for Legacy Option ROM
  - D6 No Console Output Devices are found
  - D7 No Console Input Devices are found
  - D8 Invalid password
  - D9 Error loading Boot Option(Loadimage returned error)
  - DA Boot Option is failed(Startimage returned error)
  - DB Flash update is failed
  - DC Reset protocol is not available



DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR		SPI_BIOS_ROM	
APPROVAL	BC LEE	REV	1.0		SPI_BIOS_ROM	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	16	OF 42

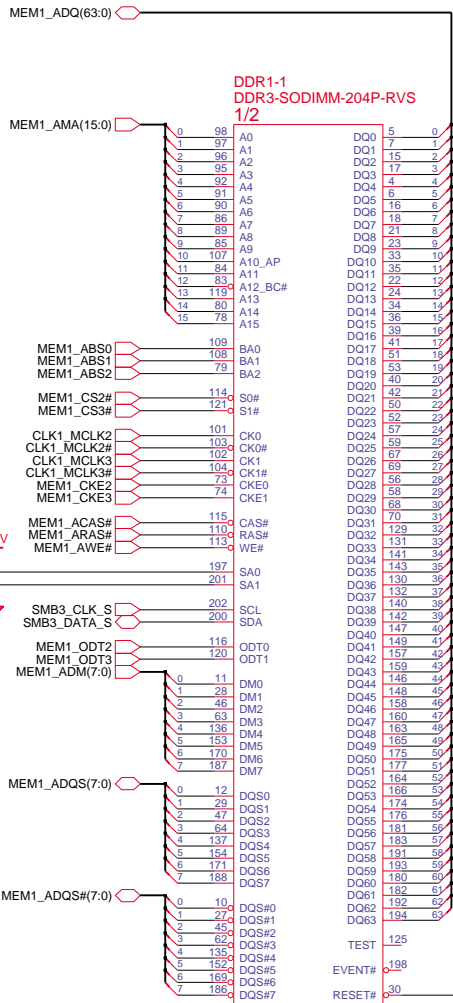


**SAMSUNG PROPRIETARY**

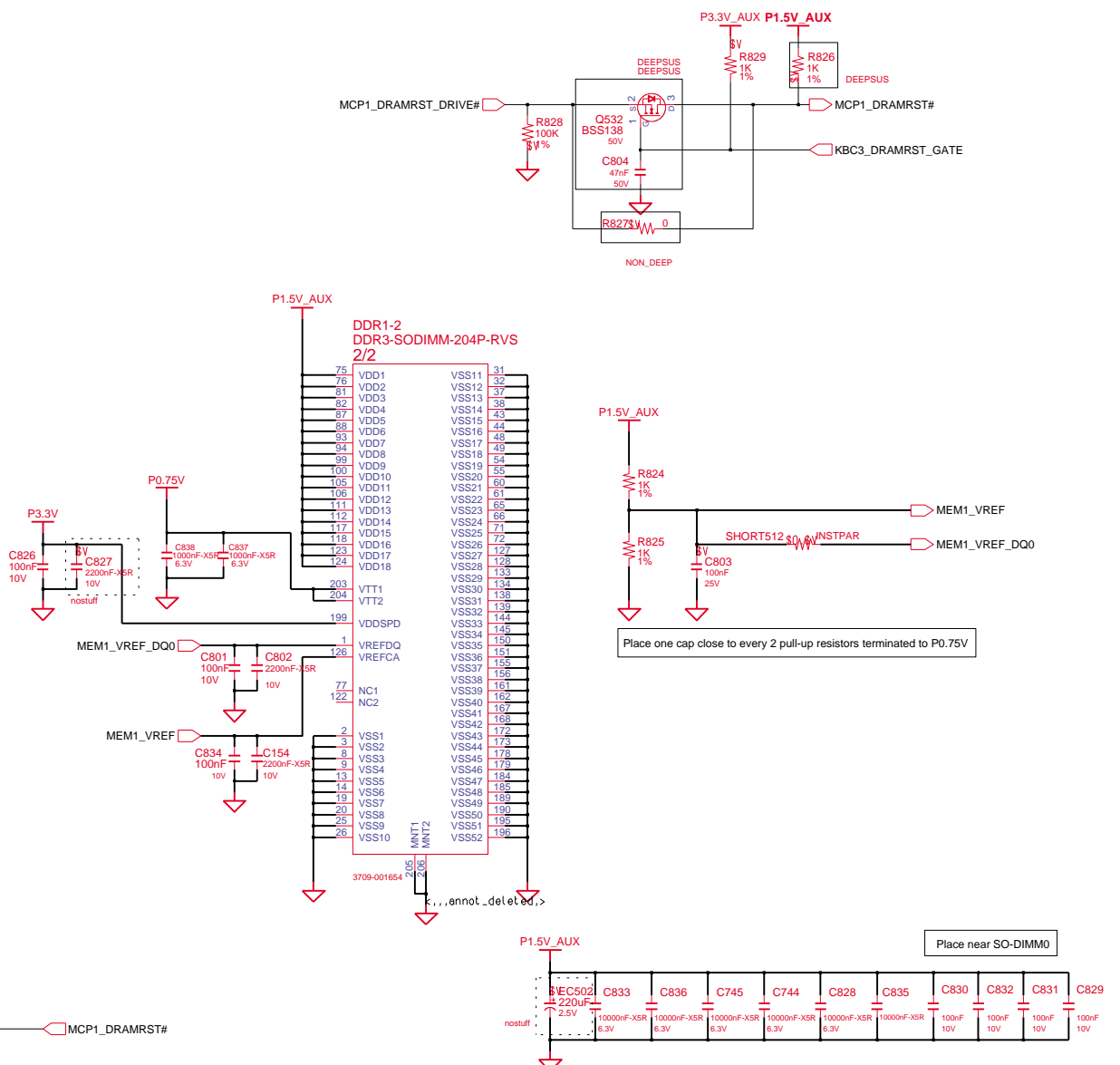
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**DDR SO-DIMM #0**

Height : 4 mm (REVERSED)



SA0	0	0
SA1	0	1
SPD ADD	0xA0	0xA2
TS ADD	0x30	0x32



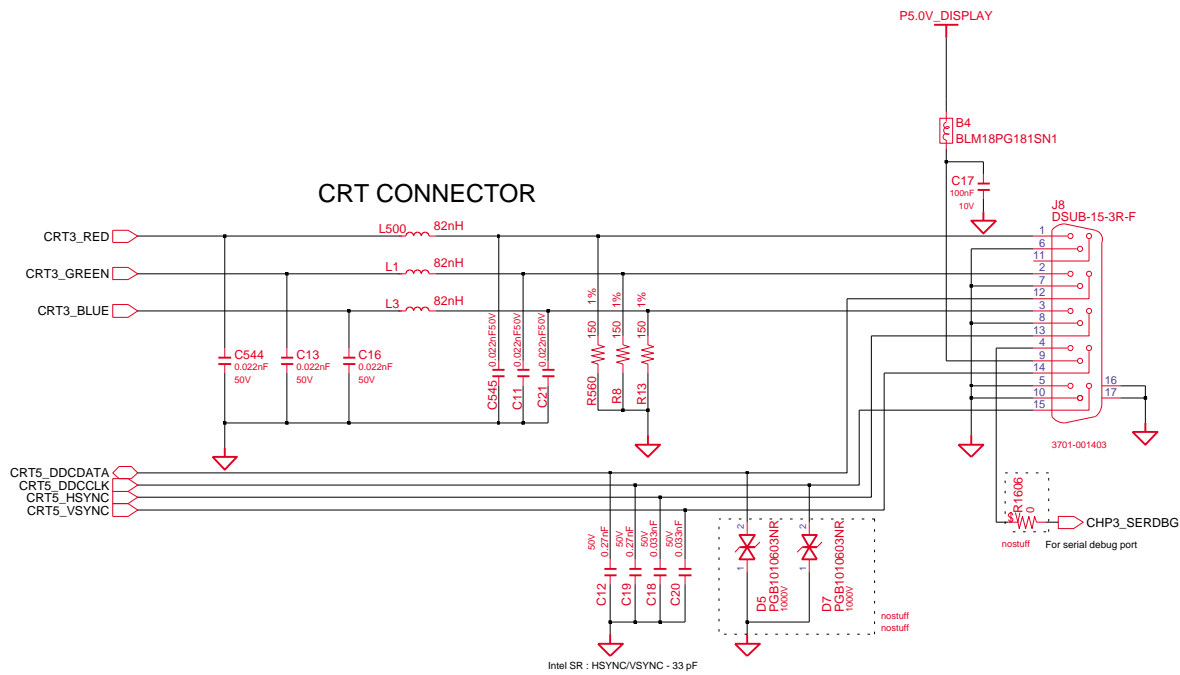
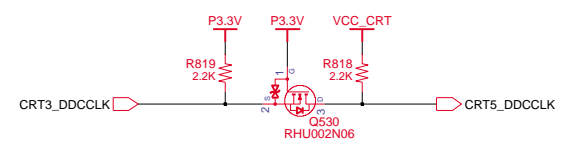
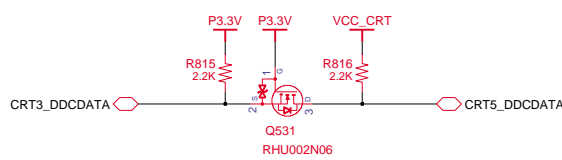
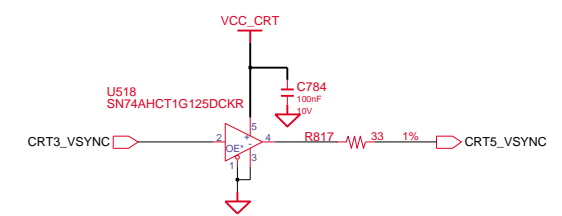
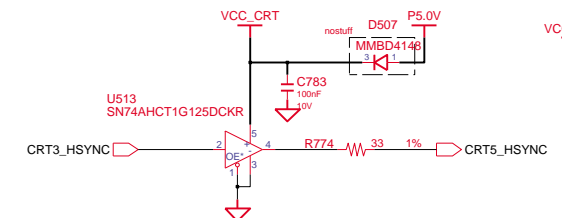
DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR	SODIMM_DDR3		
APPROVAL	BC LEE	REV	1.0	SODIMM_DDR3 #1		
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	17 OF 42	



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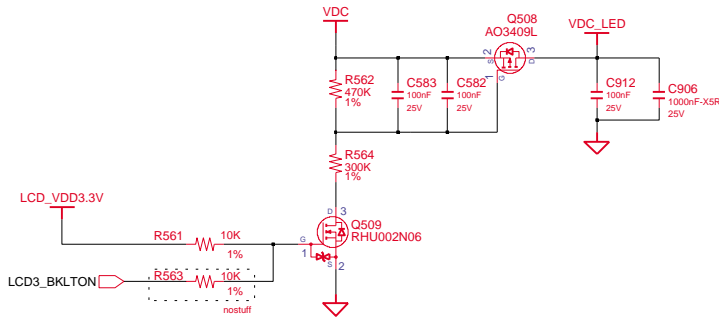
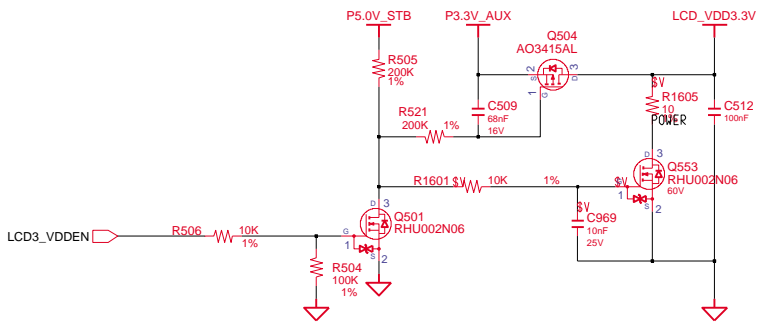
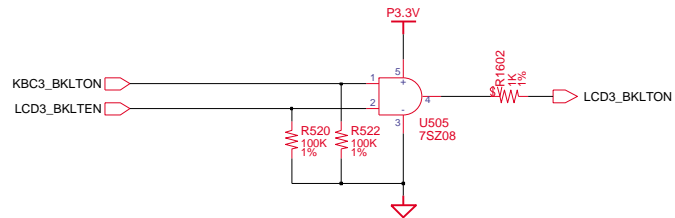
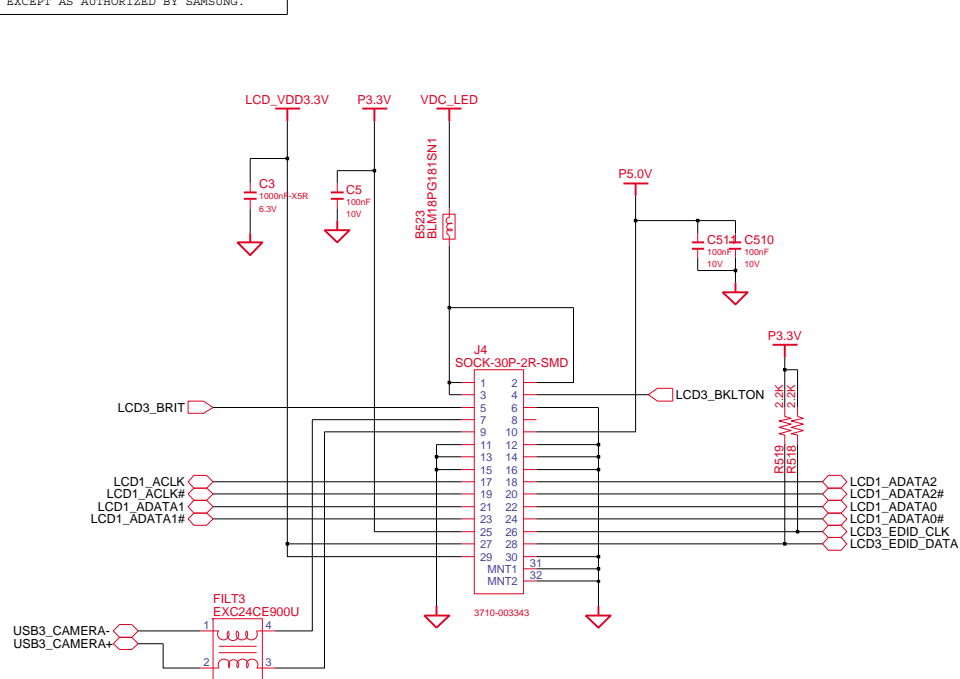
# CRT



DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	GRAPHICS_IF	PART NO.	
APPROVAL	BC LEE	REV	1.0	CRT	BA41-0XXXXA	
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	19	OF 42

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DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R GRAPHICS_IF LED LCD I/F	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	PR	PART NO.			BA41-0XXXXA
APPROVAL	BC LEE	REV	1.0	DATE			December 13, 2011 16:40:00 PM
MODULE CODE		LAST EDIT		PAGE			20 OF 42

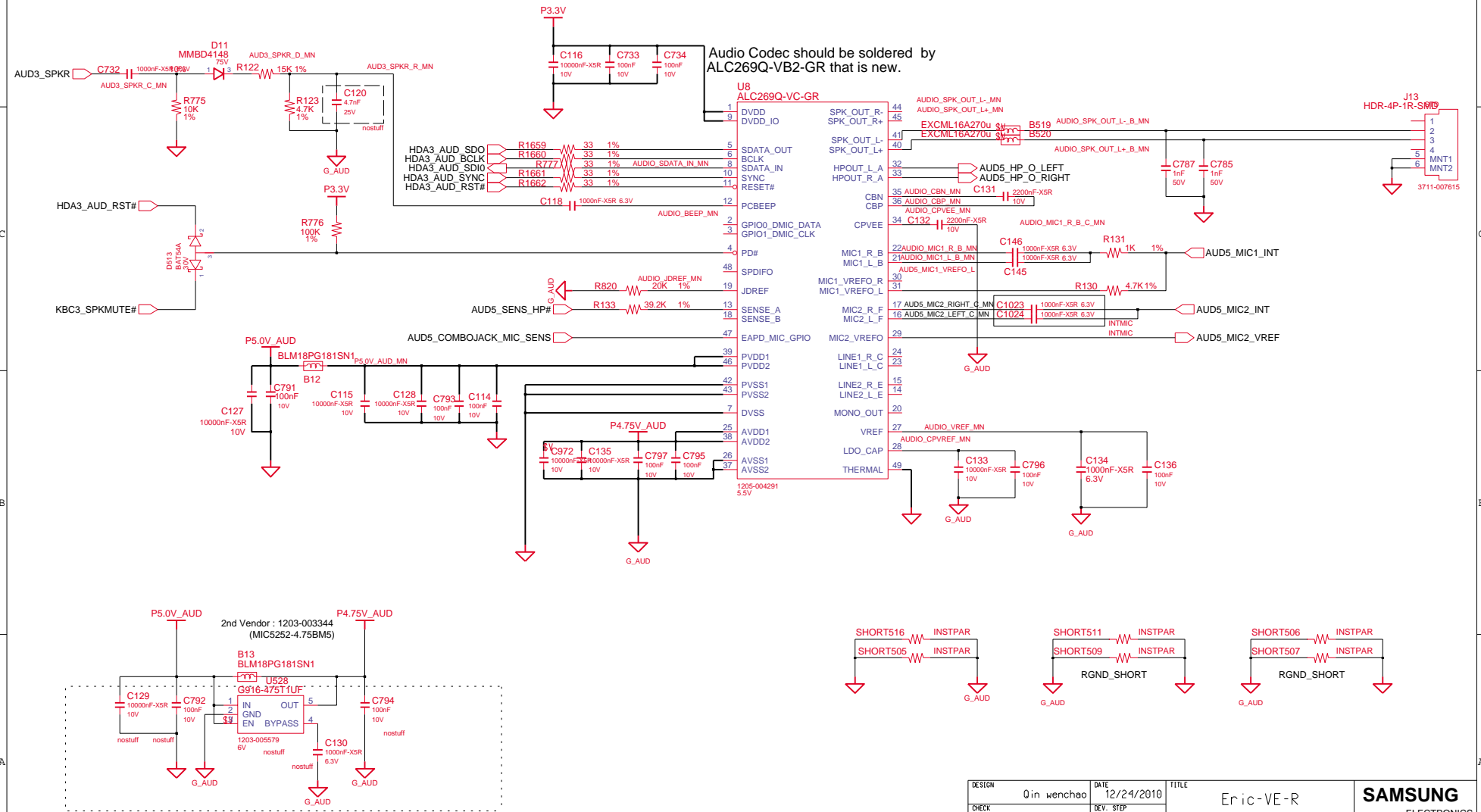


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Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

# Audio Codec



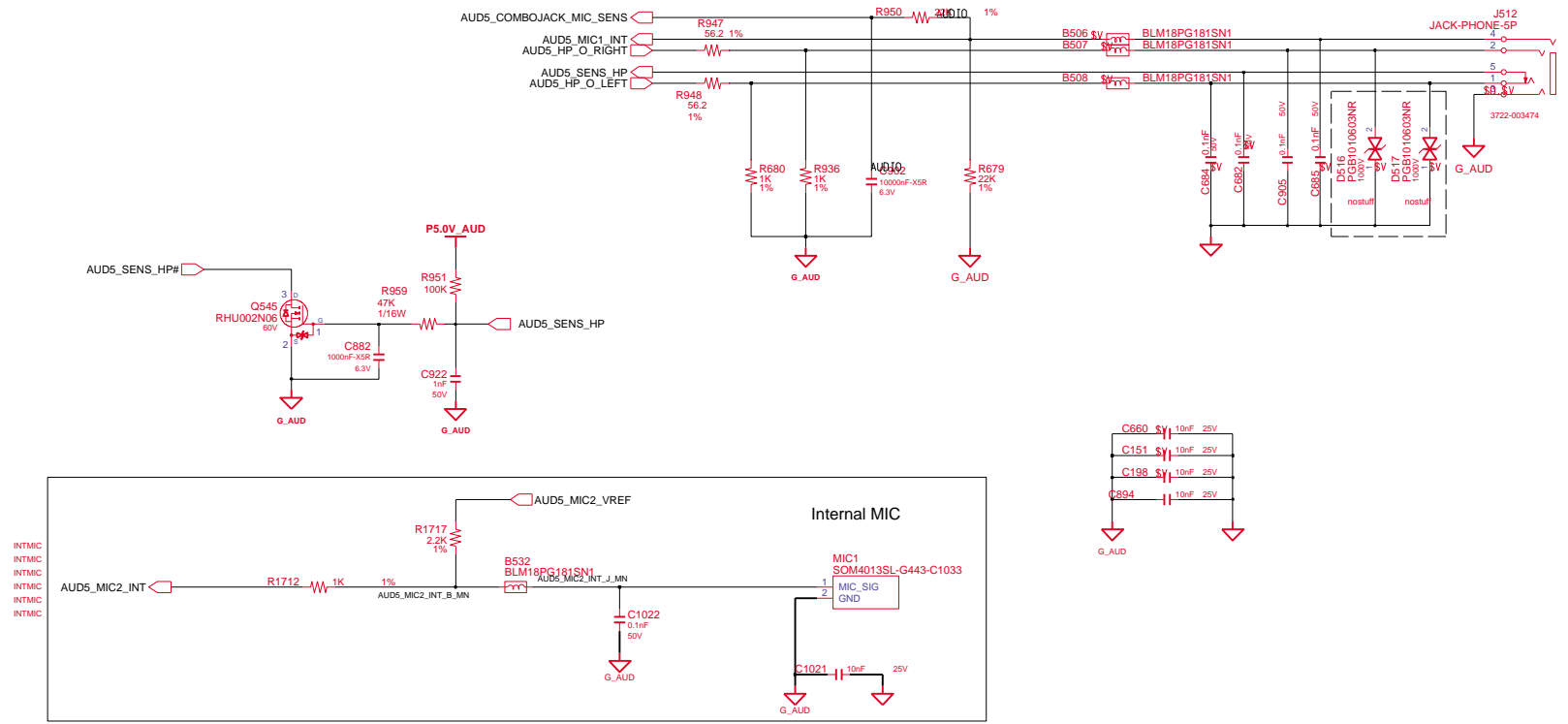
Audio Codec should be soldered by ALC269Q-VB2-GR that is new.

DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R AUDIO ALC269Q-VB	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	22 OF 42	

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# HP & MIC

Combo Jack

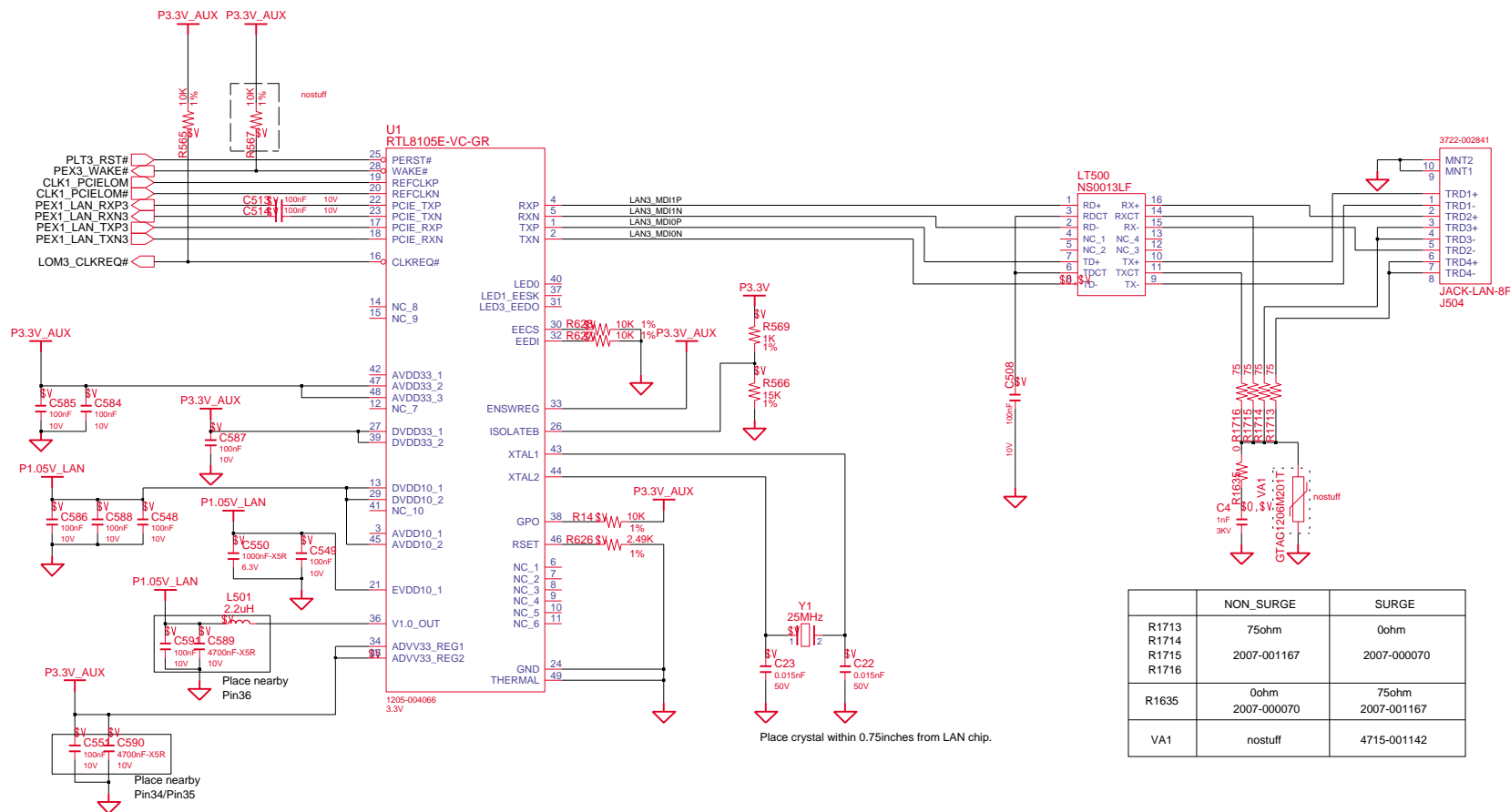


DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	REV. STEP	PR	AUDIO		
APPROVAL	BC LEE	REV	1.0	AUDIO		PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM		PAGE 23	OF 42

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# Realtek RTL8105E



	NON_SURGE	SURGE
R1713	75ohm	0ohm
R1714	2007-001167	2007-000070
R1715		
R1716		
R1635	0ohm	75ohm
	2007-000070	2007-001167
VA1	nostuff	4715-001142

Place crystal within 0.75inches from LAN chip.

DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R LAN RTL8105E	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE 24 OF 42		

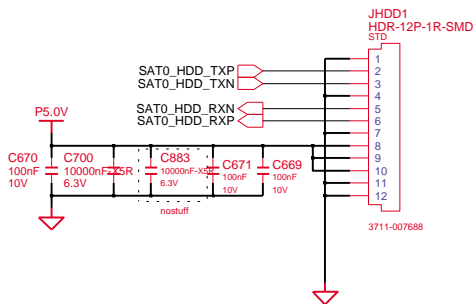


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# SATA I/F CONN

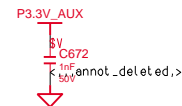
## SATA HDD CONN



For EMI



For Tx Signal at changing point of Layer



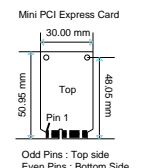
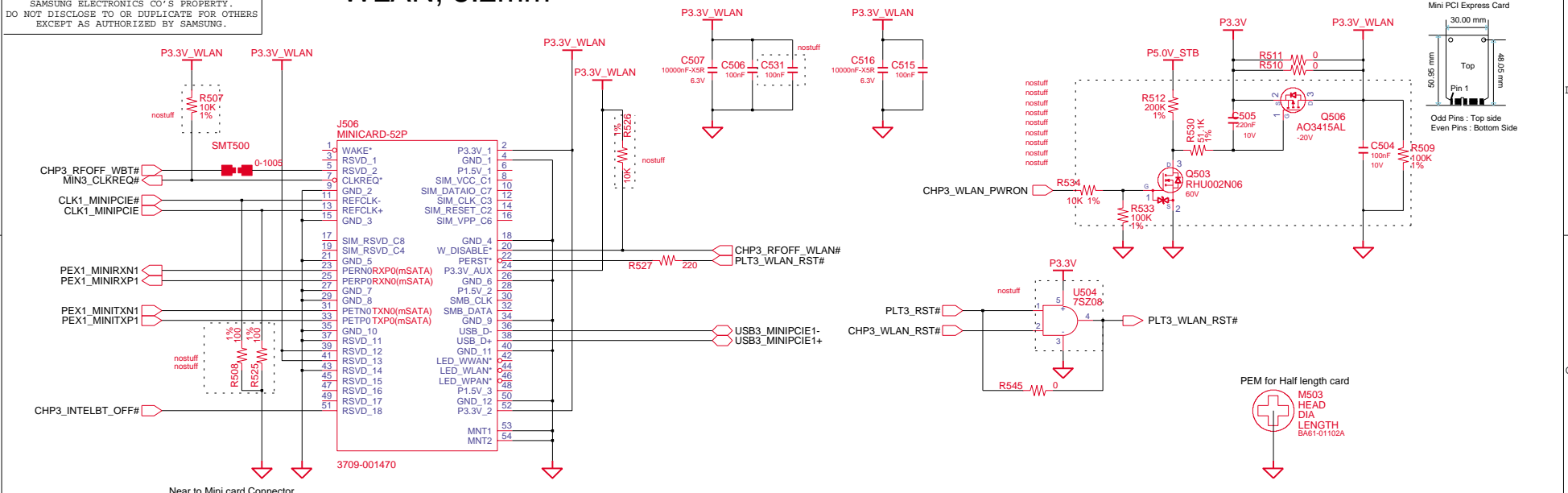
For Rx Signal at changing point of Layer

DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R SATA_DEVICES SATA I/F	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	PART NO.		
APPROVAL	BC LEE	REV	1.0	December 13, 2011 16:40:00 PM	PAGE	25 OF 42
MODULE CODE		LAST EDIT				

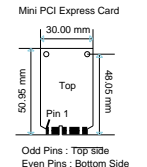
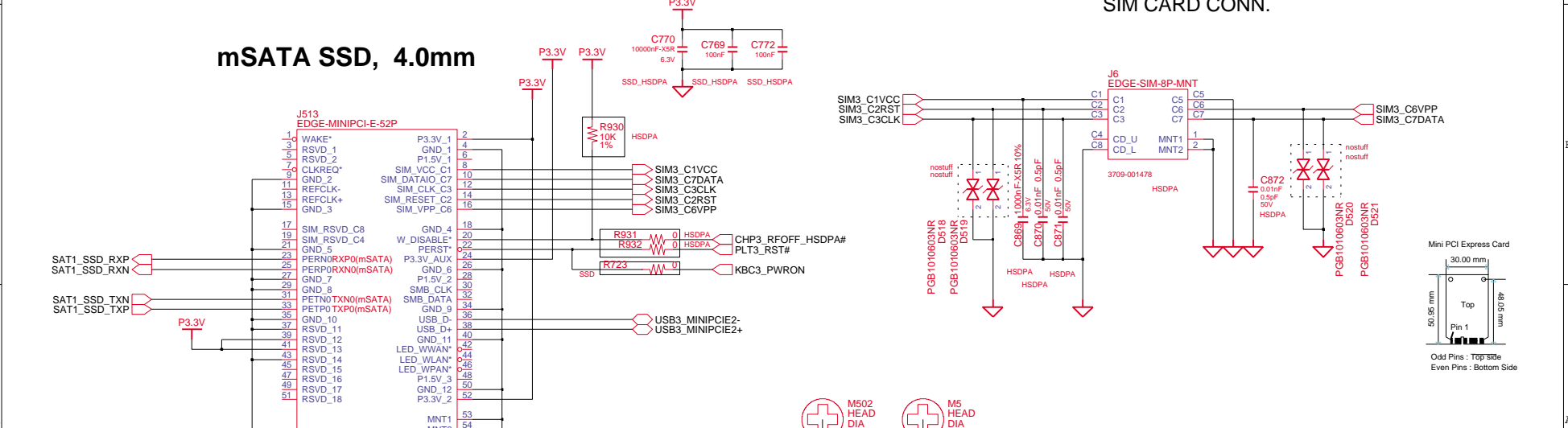
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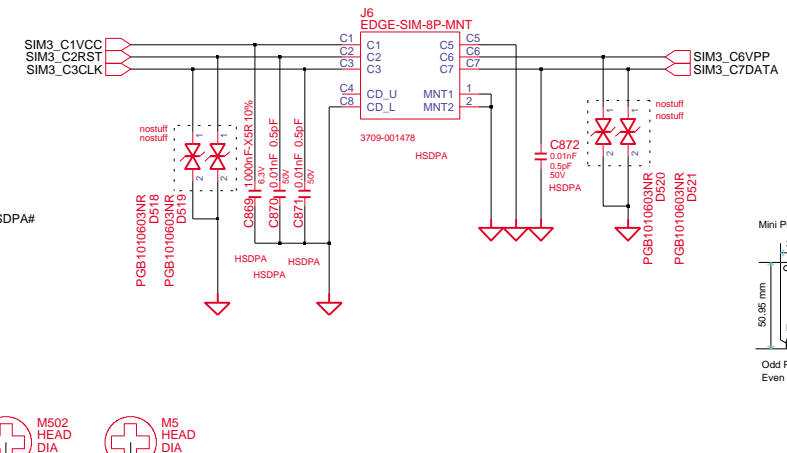
# WLAN, 5.2mm



# mSATA SSD, 4.0mm



# SIM CARD CONN.

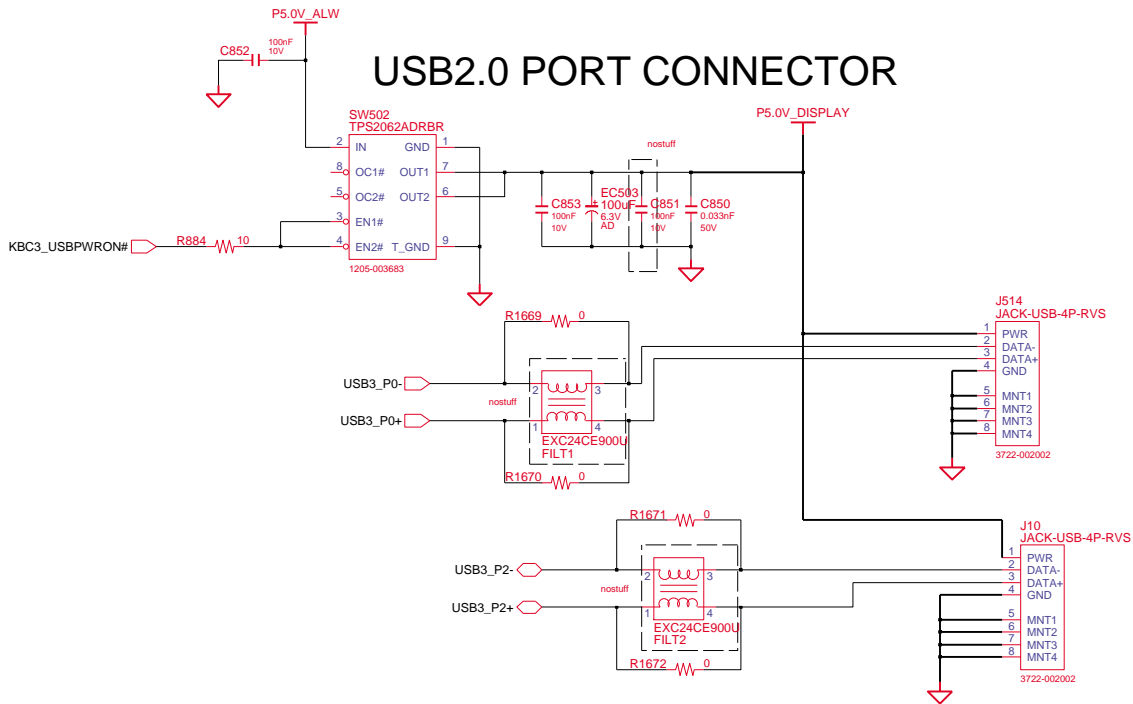


DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R MINI_PCIE_CONN	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR	REV	1.0	
APPROVAL	BC LEE	LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	26	OF 42

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# USB2.0 PORT CONNECTOR

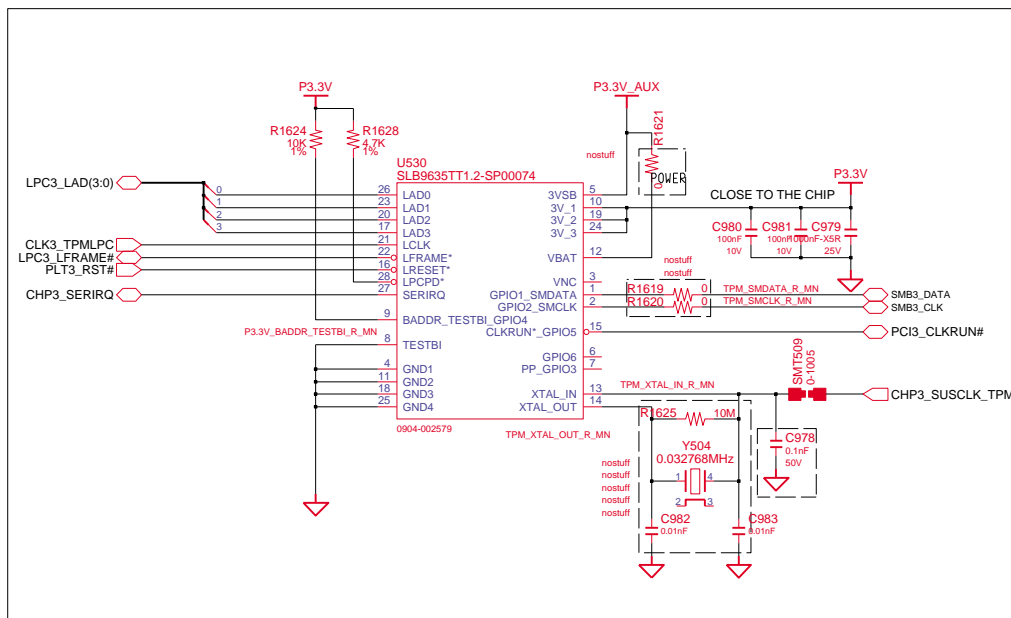


DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R USB_CONN USB PORT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	27	OF 42

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**TPM 1.2(Option.)**



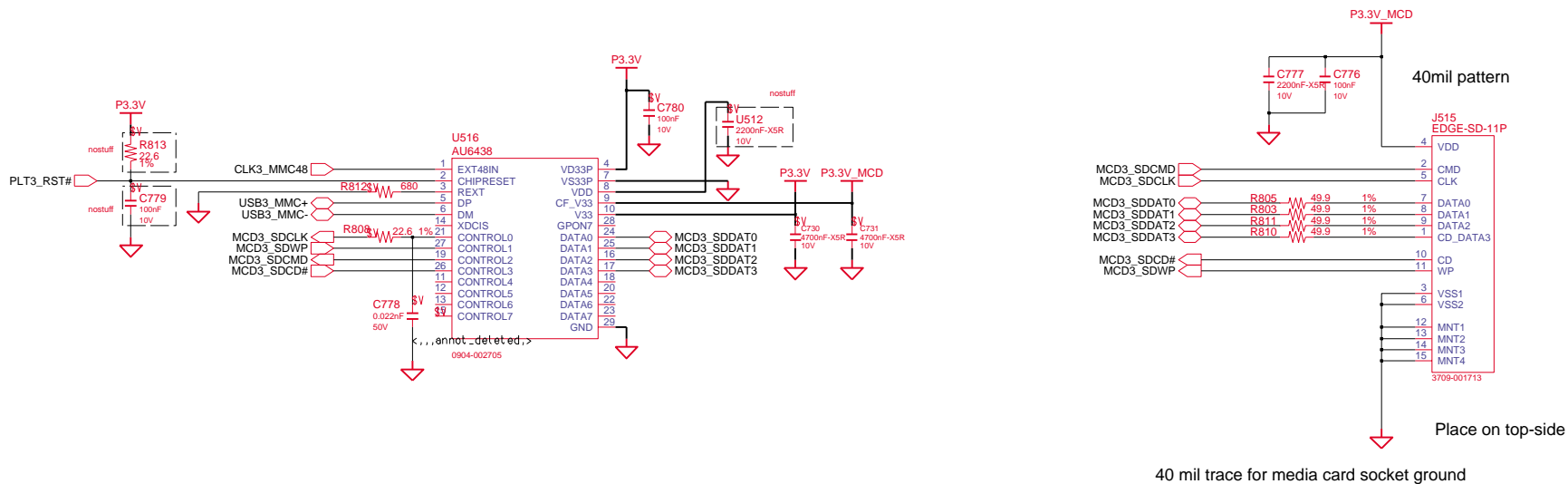
TPM  
TPM  
TPM  
TPM  
TPM  
TPM

DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	USB_DEVICES SB I/F	TPM	
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	28	OF 42

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# MMC(AU6438)



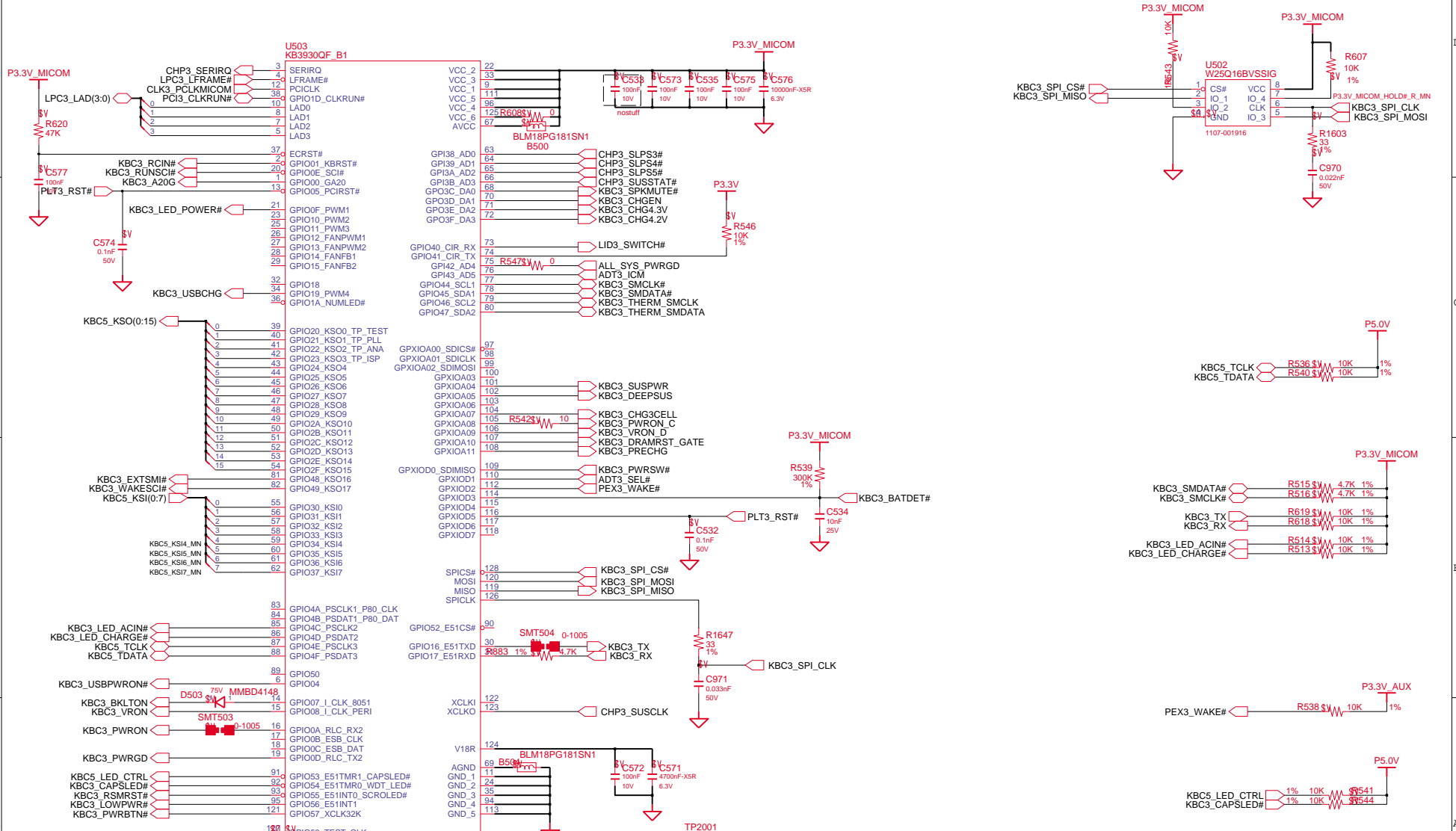
DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shiji	DEV. STEP	PR		MMC	
APPROVAL	BC LEE	REV	1.0		AU6437	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	29	OF 43

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# MAIN BOARD (MICOM 3930)

BE CAUTION SPI ROM SIZE!!

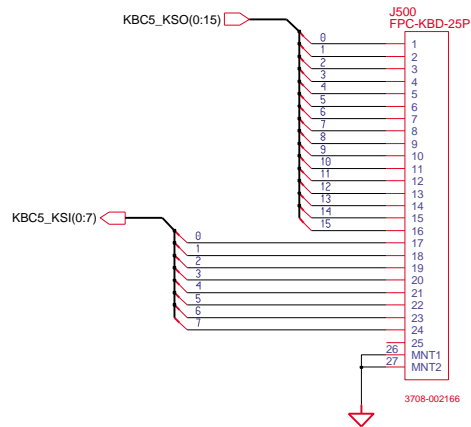


DESIGN	Qin wenchao	DATE	01/08/2009	TITLE	Eric-VE-R	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	MICOM	MICOM	
APPROVAL	BC LEE	REV	1.0	MICOM	MICOM	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	30	OF 42

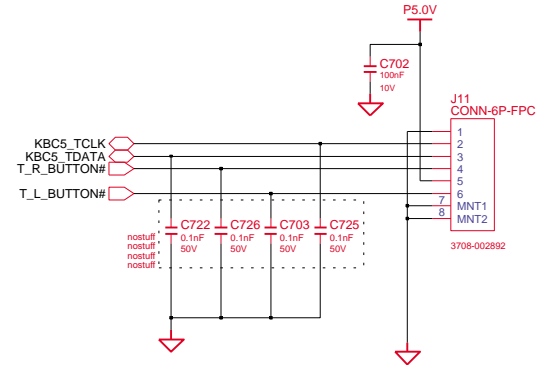
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# Micom Glue Logic

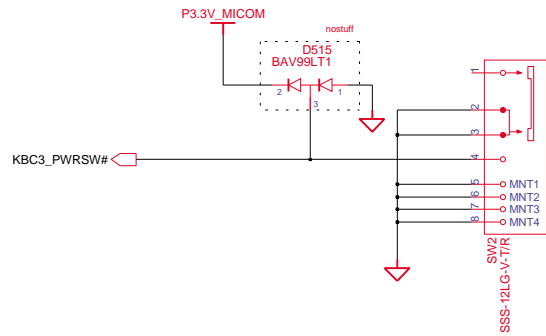
## KEYBOARD



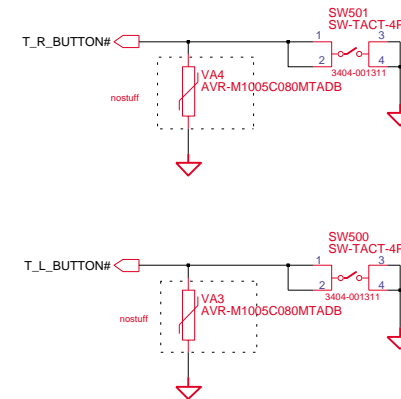
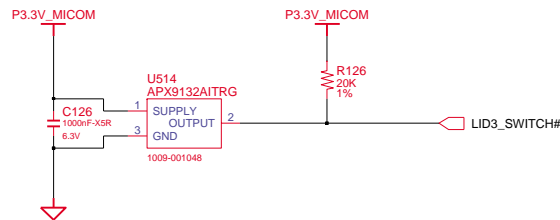
## TOUCHPAD



## Power Slide Switch



## LID SWITCH

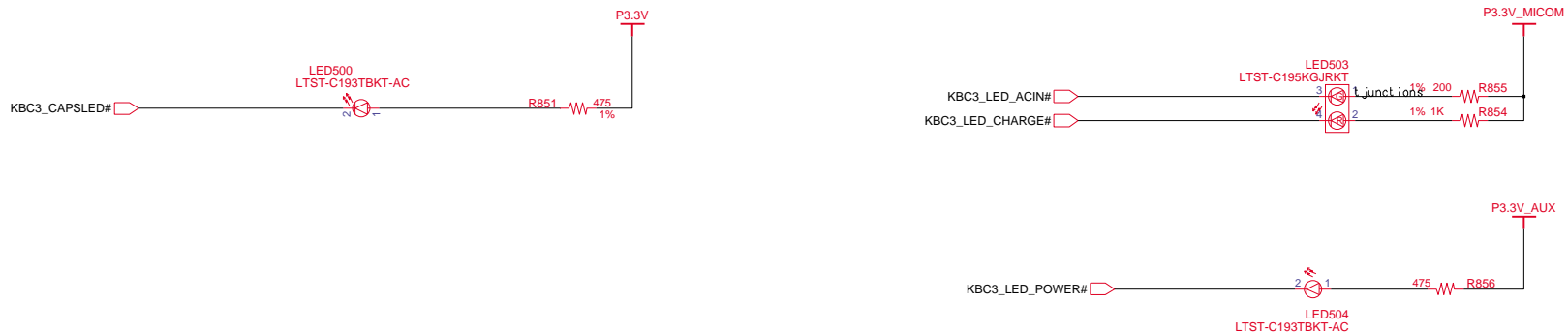


DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R MICOM MICOM GLUE LOGIC	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	31	OF 42

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# LED SWITCH LOGIC



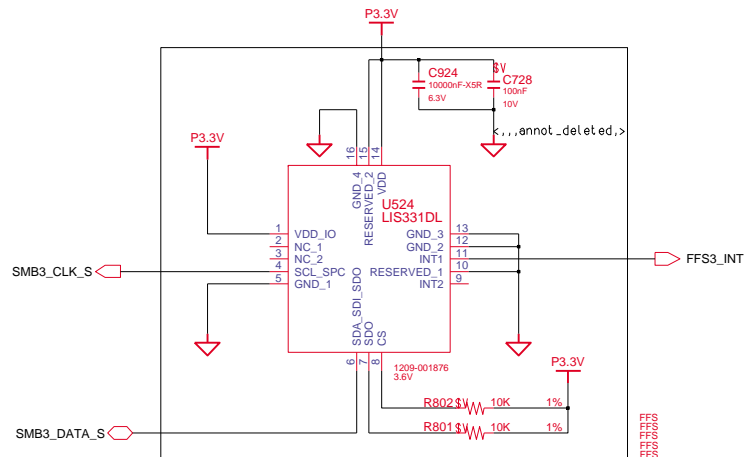
DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R LED_Switch LED_Switch	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	PR	PART NO.			BA41-0XXXXA
APPROVAL	BC LEE	REV	1.0	PAGE			32 OF 42
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM				



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**FREE FALL SENSOR**

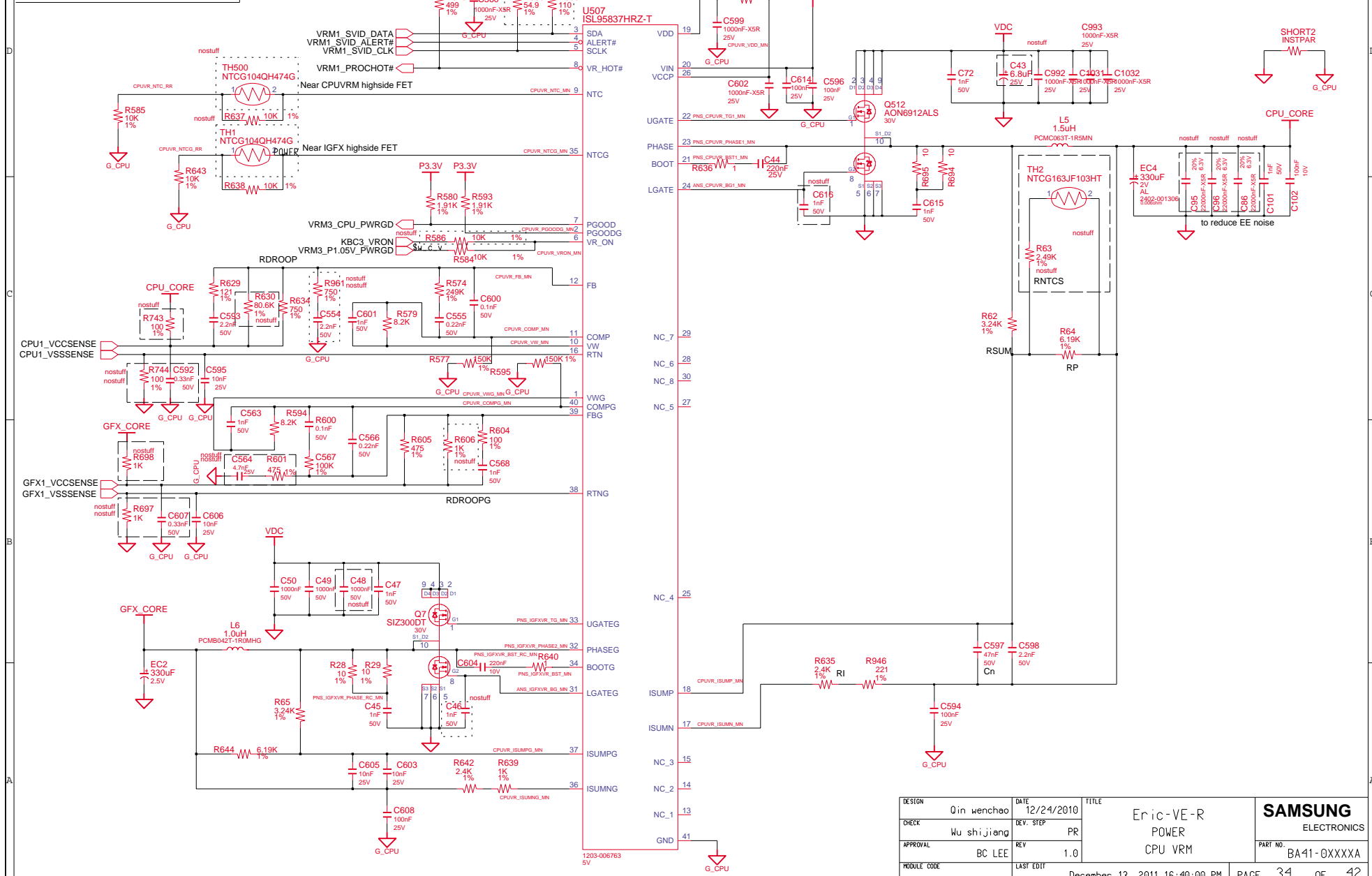


DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R FFS FreeFallSensor	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	PART NO.		
APPROVAL	BC LEE	REV	1.0	LAST EDIT	December 13, 2011 16:40:00 PM	PAGE 33 OF 42
MODULE CODE	undefined					

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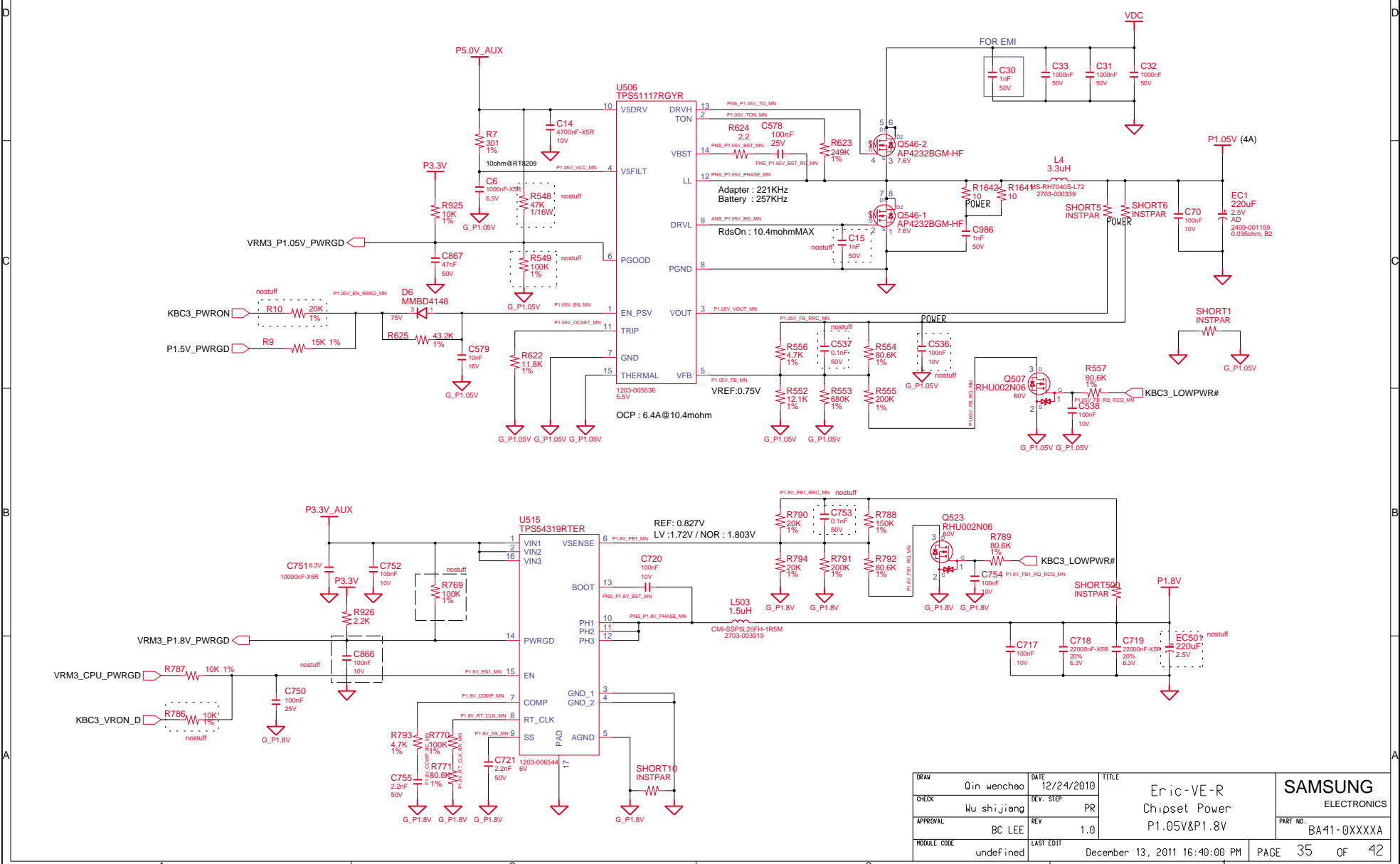
**CPU VRM ( Ceder trail M [IMVP-7] )**



DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R POWER CPU VRM	<b>SAMSUNG</b> ELECTRONICS PART NO. BA14-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	34 OF 42	

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# Chipset Power ( P1.8V & P1.05V )

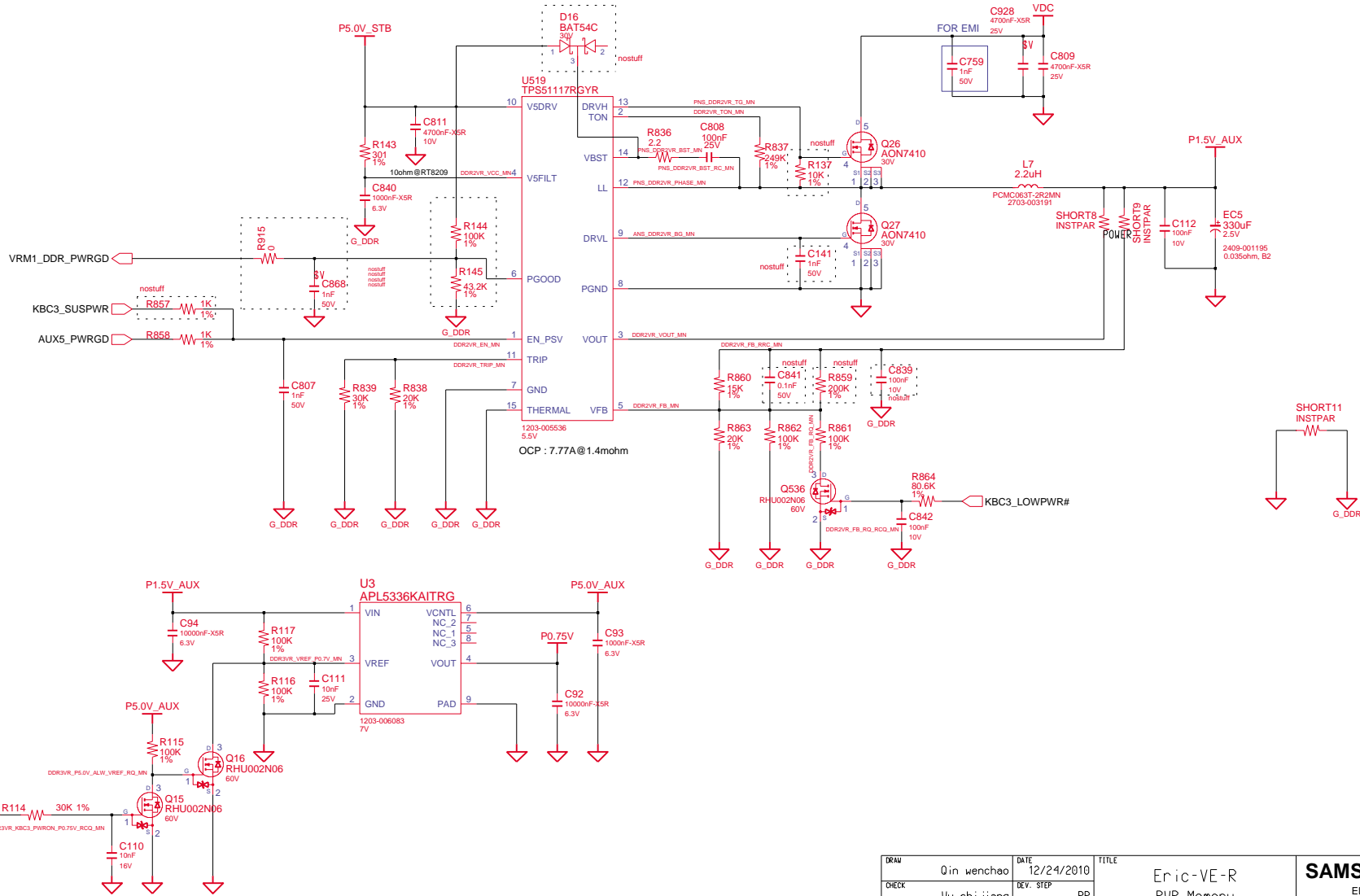


DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R Chipset Power P1.05V&P1.8V	<b>SAMSUNG</b> ELECTRONICS PART NO. BA11-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	35 OF 42	

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# DDR3 Power ( P1.5V\_AUX & P0.75V )

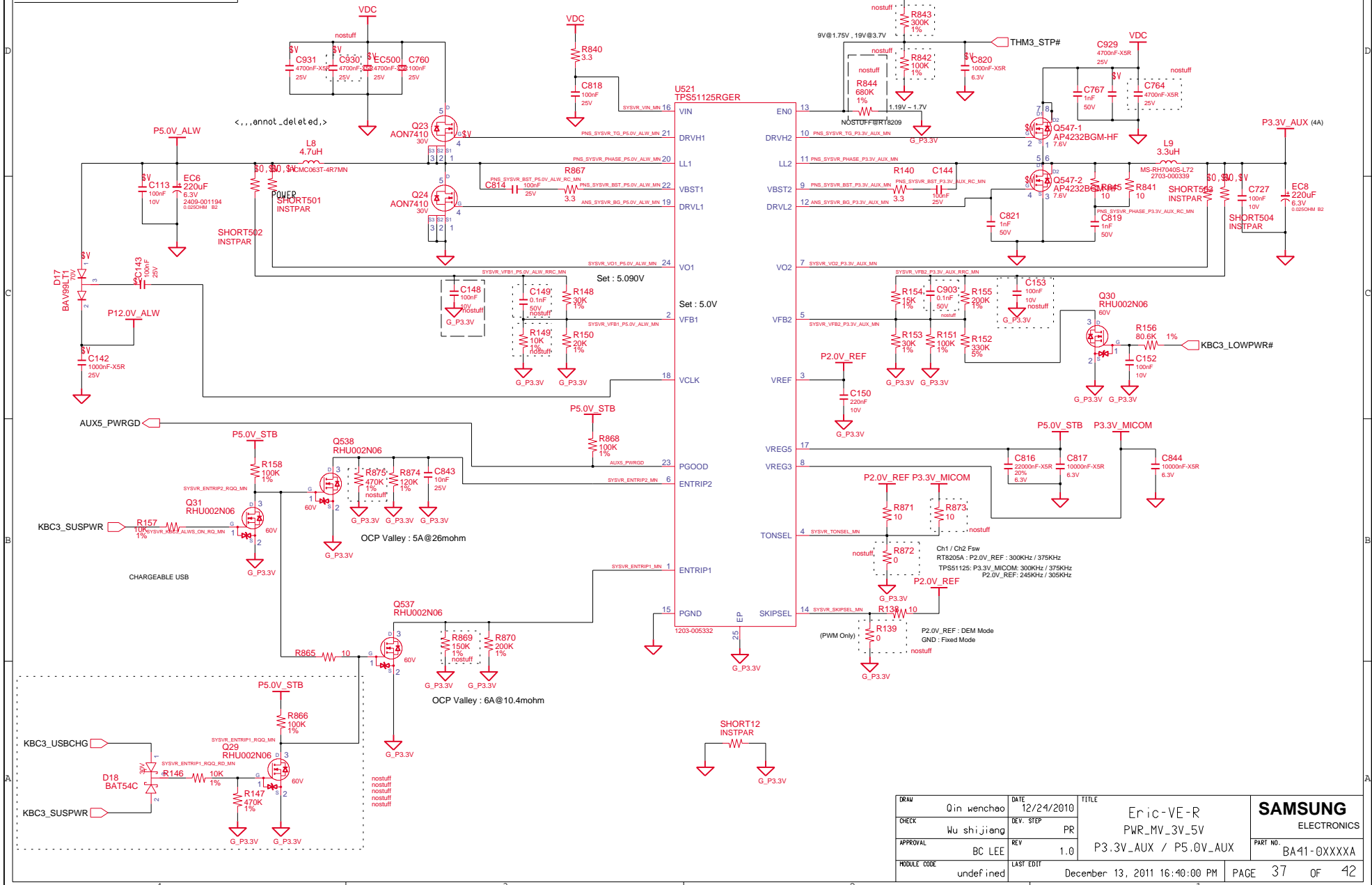


DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R PWR.Memory P1.5V_AUX&P0.75V	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	PART NO.		
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	36	OF 42

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# P3.3V\_AUX & P5.0V\_ALW

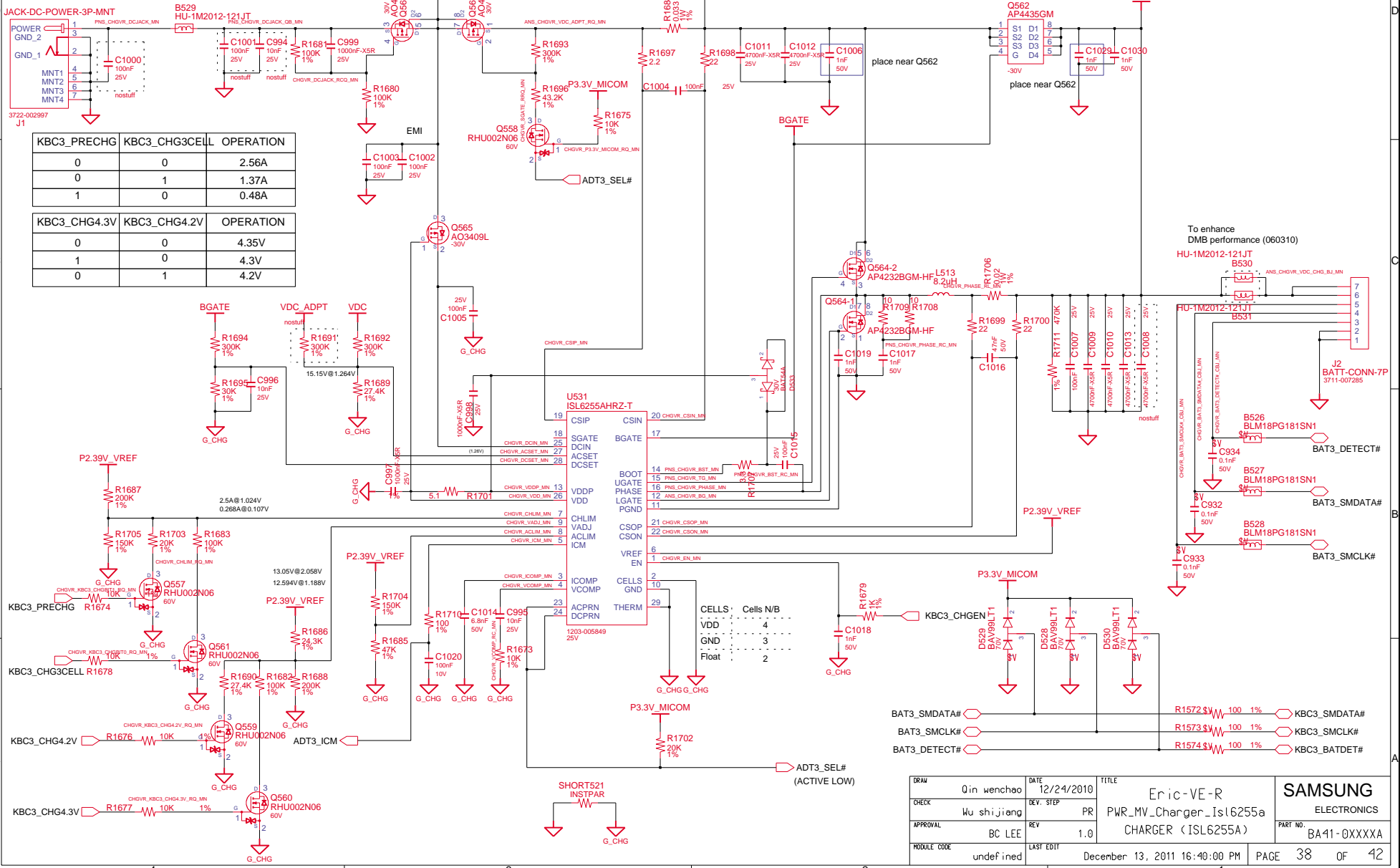


DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R PWR_MV_3V_5V	<b>SAMSUNG</b> ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	P3.3V_AUX / P5.0V_AUX		
APPROVAL	BC LEE	REV	1.0	PART NO. BA41-0XXXXA		PAGE 37 OF 42
MODULE CODE	undefined	LAST EDIT	December 13, 2011 16:40:00 PM			

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# CHARGER & POWER MANAGEMENT

VCHG=12.597V@2600Cell  
 VCHG=13.05V@2950Cell  
 ICHG=2.56A FOR 5200mAh & 4000mAh



KBC3_PRECHG	KBC3_CHG3CELL	OPERATION
0	0	2.56A
0	1	1.37A
1	0	0.48A

KBC3_CHG4.3V	KBC3_CHG4.2V	OPERATION
0	0	4.35V
1	0	4.3V
0	1	4.2V

CELLS	Cells N/B
VDD	4
GND	3
Float	2

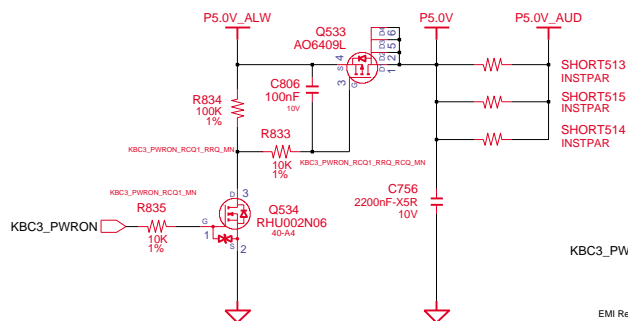
DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R	SAMSUNG ELECTRONICS
CHECK	Wu shijiang	DEV. STEP	PR	PWR_MV_Charger_Isl6255a	CHARGER (ISL6255A)	
APPROVAL	BC LEE	REV	1.0			PART NO. BA11-0XXXXA
MODULE CODE	undefined	LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	38	OF 42



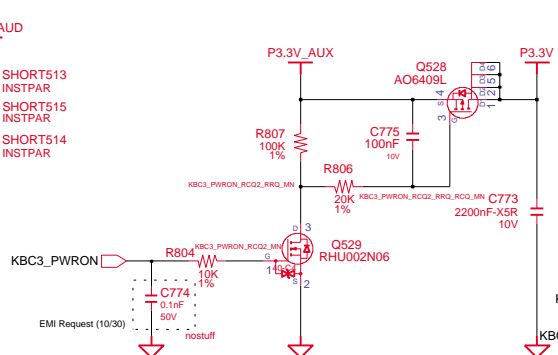
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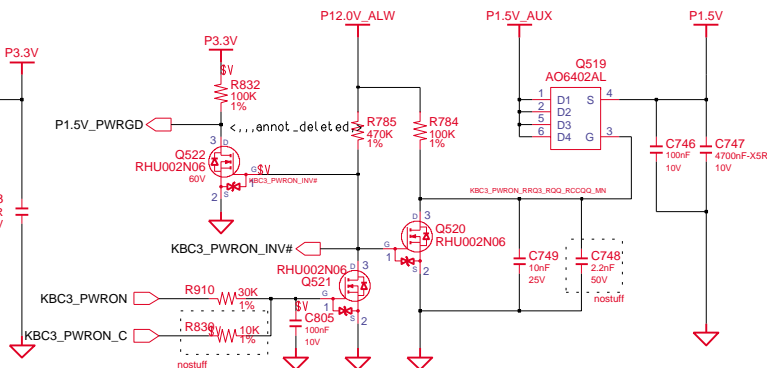
### Load Switch Control (P5.0V)



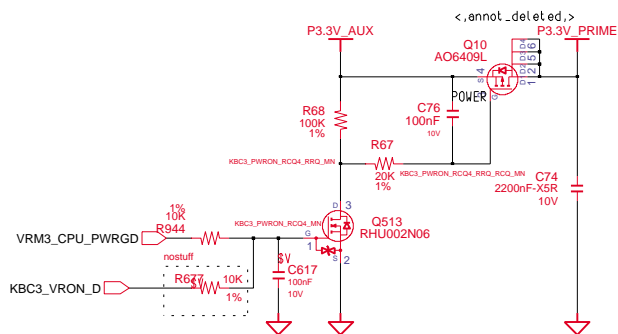
### Load Switch Control (P3.3V)



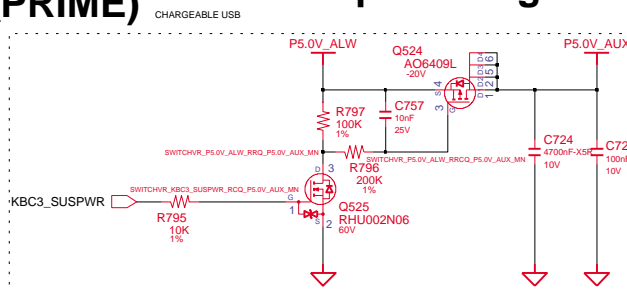
### Load Switch Control (P1.5V)



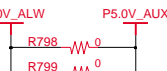
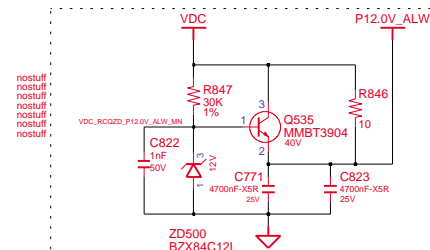
### Load Switch Control (P3.3V\_PRIME)



### Sleep'n Charger



### P12V\_ALW



For Non-CHARGEABLE USB

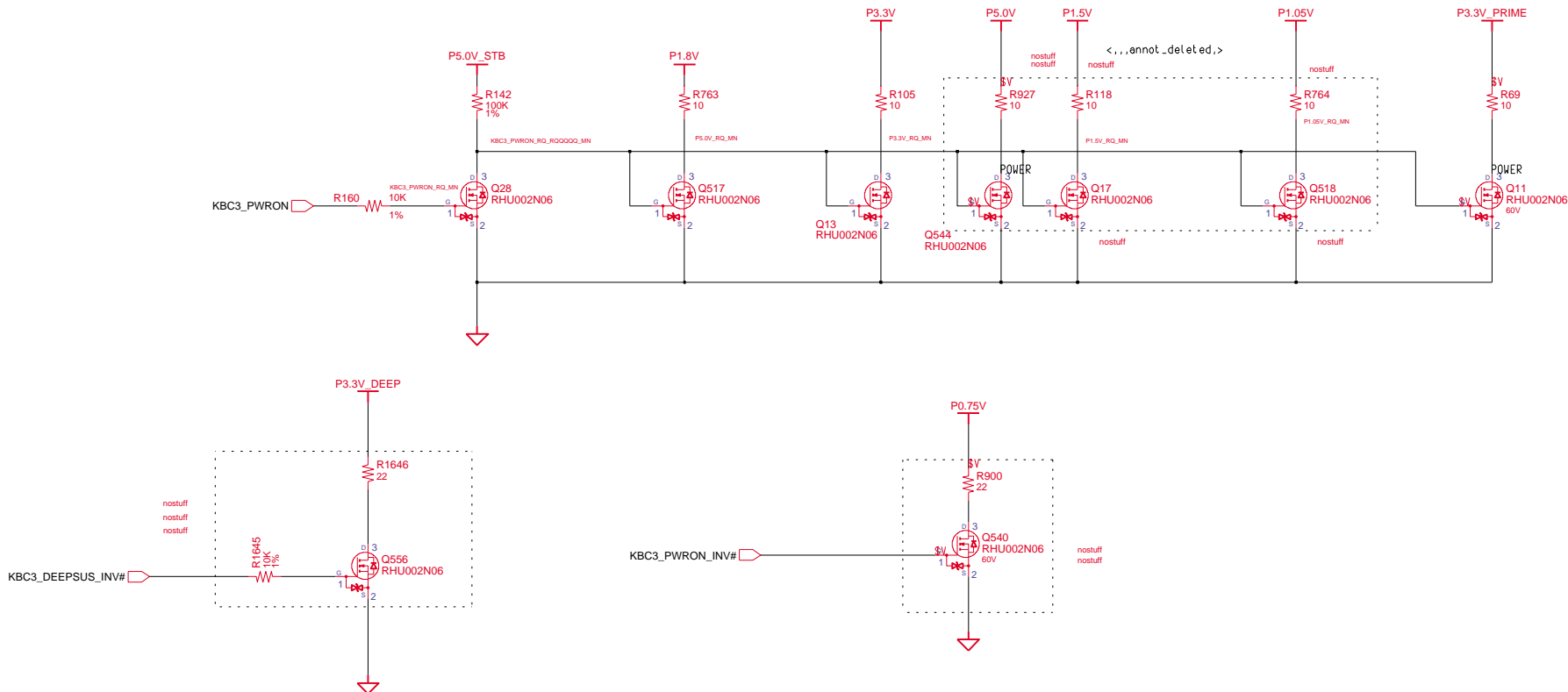
DESIGN	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR		Switched PWR	
APPROVAL	BC LEE	REV	1.0		Switched PWR	
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE	40 OF 42	



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# PWR Discharger



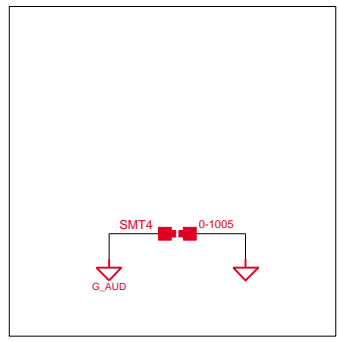
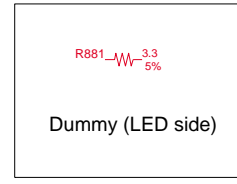
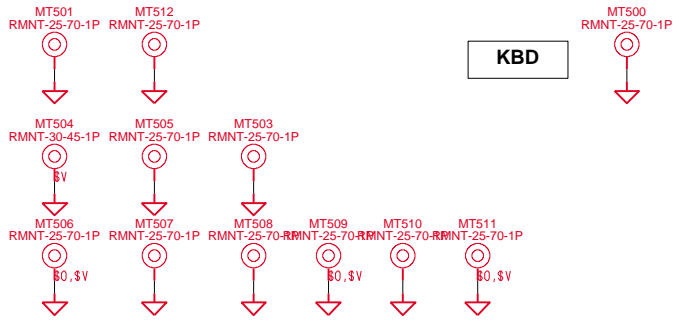
DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R Discharger Discharger	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-0XXXXA
CHECK	Wu shijiang	DEV. STEP	PR			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE 41 OF 42		

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**Top + Bottom  
 (Bottom side)**

**KBD**

**M/B  
 +  
 Top**



FOR EMI

**Multi\_assy Description**

Multi_assy	Description
HDMI	for sku with HDMI
NON_HDMI	for sku without HDMI
DEEPSUS	for sku with deep S3 function
NON_DEEP	for sku without deep S3 function
FFS	for sku with free fall sensor
NON_FFS	for sku without free fall sensor
HSDPA	for sku with HSDPA
NON_HSDPA	for sku without HSDPA
FULL_HSDPA	for full HSDPA screw
HALF_HSDPA	for half HSDPA screw
TPM	for BIOS detect there is TPM
NON_TPM	for BIOS detect there is no TPM
SSD	for sku with in-card SSD
ISSD	for sku with onboard SSD
SSD_HSDPA	for the connector that SSD & HSDPA common use
P12_18	for P5 SSD surport
SMSC	for sku with SMSC thermal sensor
GMT	for sku with GMT thermal sensor
INTMIC	for BIOS detect there is internal MIC
NON_INTMIC	for BIOS detect there is no internal MIC
HDD	for sku with HDD
SSD	for sku with SSD

DRAW	Qin wenchao	DATE	12/24/2010	TITLE	Eric-VE-R ETC MOUNT & MULTI-ASSY	<b>SAMSUNG</b> ELECTRONICS	
CHECK	Wu shijiang	DEV. STEP	PR				
APPROVAL	BC LEE	REV	1.0	PART NO.			BA41-0XXXXA
MODULE CODE		LAST EDIT	December 13, 2011 16:40:00 PM	PAGE			42 OF 42