

Compal Confidential

NIWE2

Schematics Document

Arrandale

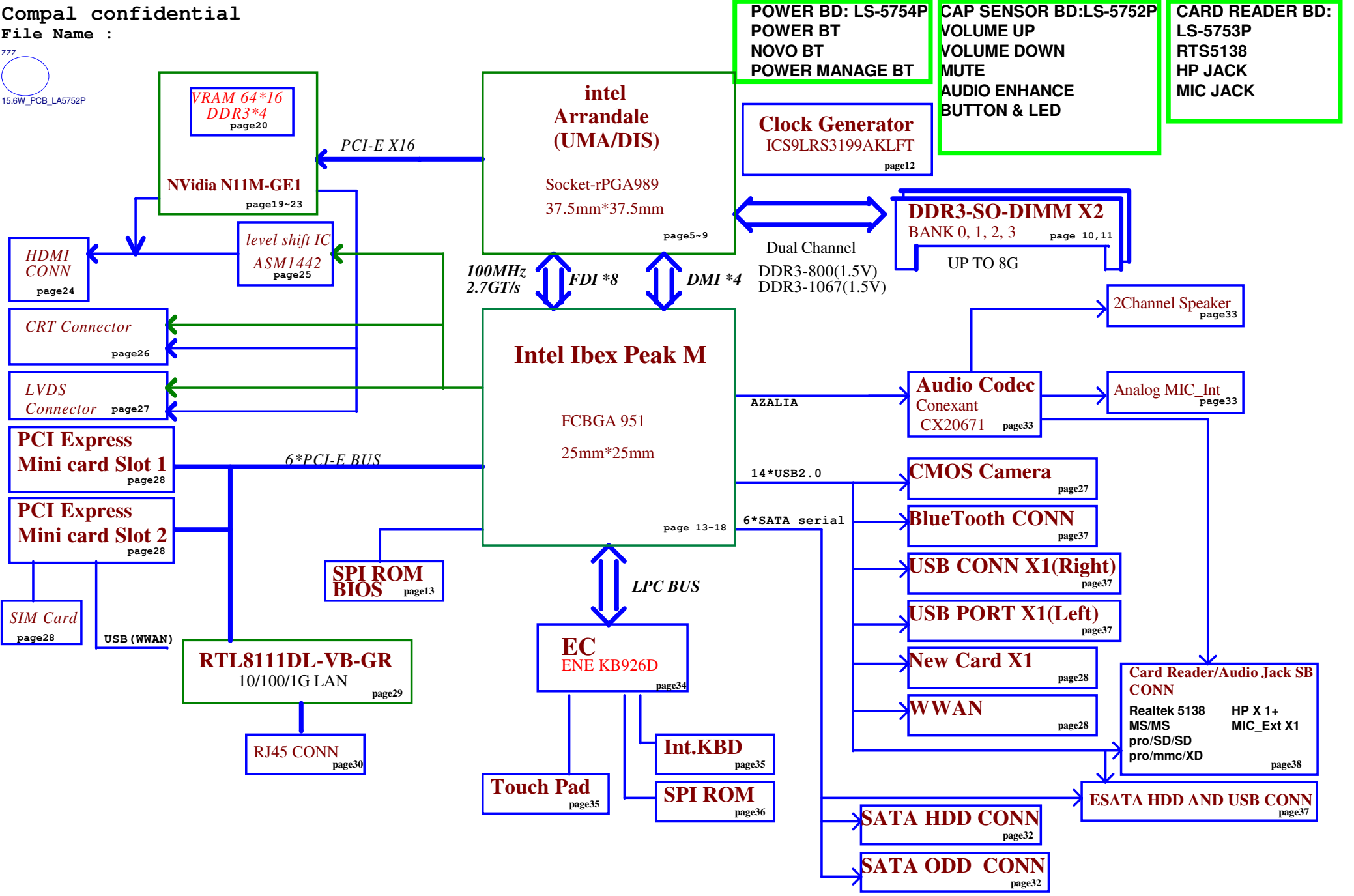
with Intel IBEX PEAK-M core logic

REV: 0.3

Security Classification	Compal Secret Data			<i>Compal Electronics, Ltd.</i>		
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title Cover Sheet		
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				Date: Thursday, October 29, 2009		



15.6W_PCB_LA5752P



Security Classification	Compal Secret Data			Title		
Issued Date	2008/03/24	Deciphered Date	2008/04/	Compal Electronics, Inc.		
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				Custom	LA-5752P	0.3
				Date:	Thursday, October 29, 2009	Sheet 2 of 51

Compal Electronics, Inc.

MB Block Diagram

LA-5752P

Thursday, October 29, 2009 Sheet 2 of 51

DDR3 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS
				State
S0	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

	EVT	NON-USE
45@	(45 BOM)	
100@	10/100 LAN	
GIGA@	GIGA LAN	
UMA HDMI@	FOR UMA HDMI components	
HDMI@	FOR HDMI components	
3G@	3G(WWAN) function	
X76@	(X76 BOM)	
ESATA@	ESATA function	
CMOS@	Camera function	
BT@	Blue Tooth	
10M@	FOR 10M CHIP	
11M@	FOR 11M CHIP	
UMA@	UMA only (Arranddale)	
DIS@	DIS only (Arranddale)	
VGA@	FOR NVIDIA PART	
HYBRID@	FOR SWITCHABLE	
HU@	SWITCHABLE or UMA only	
HD@	SWITCHABLE or DIS only	

SKU

Arrandale (dGPU) DIS only	DIS@ / 100@ for EVT
Arrandale (iGPU) UMA only	UMA@ / 100@ for EVT
Arrandale (iGPU+dGPU) SWITCHABLE	VGA@+HD@+HU@+HYBRID@

PCIe PORT LIST

PORT	DEVICE
1	
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	
7	
8	

USB PORT LIST

PORT	DEVICE
0	RIGHT SIDE
1	LEFT SIDE
2	CMOS
3	LEFT SIDE
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	
10	NEW CARD
11	BT
12	
13	3G

VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID or Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6 GPIO5 N10M-GS N10P-GS

GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	0	0.9V	0, 10
1	1	1.0V (N10M-GS) 0.925V (N10P-GS)	

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

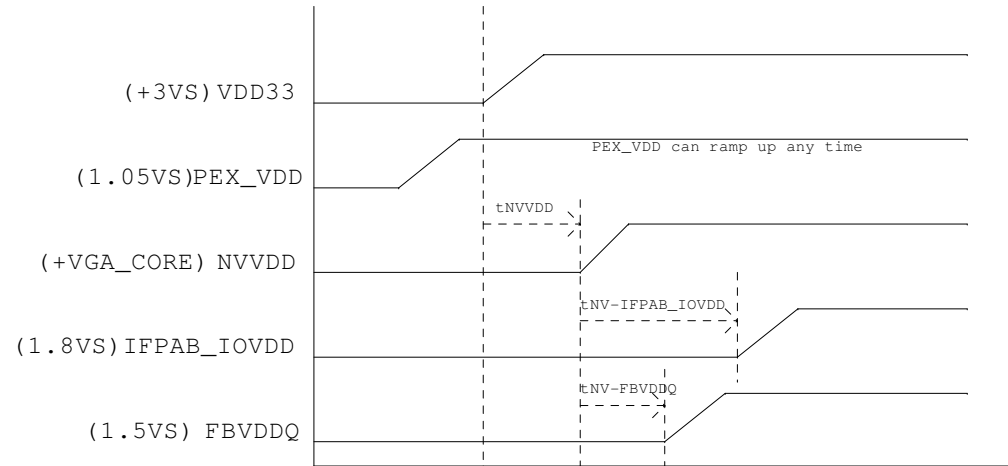
Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (mA)		I/O and PLLVDD (1.8V) (mA)		I/O and PLLVDD (1.05V) (mA)		Other (3.3V) (mA)	
				(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.5V) (W)		FBVDDQ (GPU+Mem) (1.5V) (W)		PCI Express (1.05V) (6) (mA)		I/O and PLLVDD (1.8V) (mA)		I/O and PLLVDD (1.05V) (mA)		Other (3.3V) (mA)	
				(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

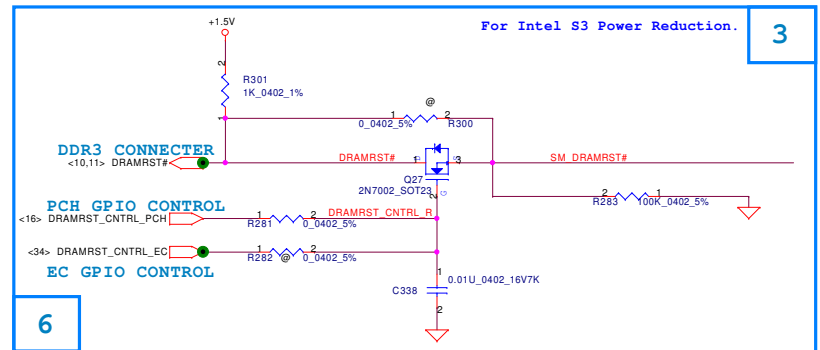
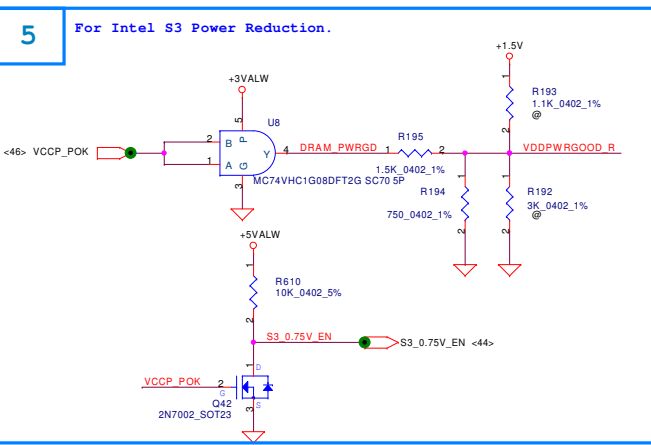
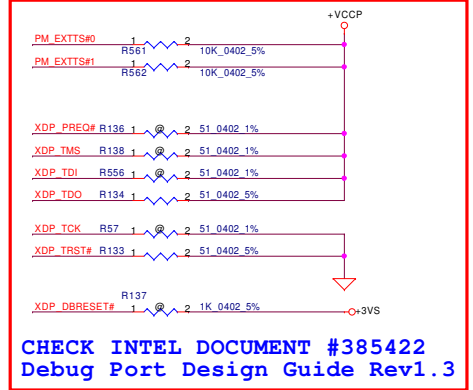
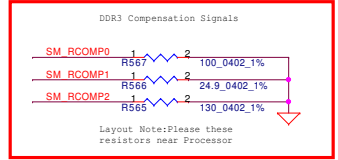
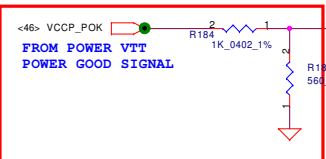
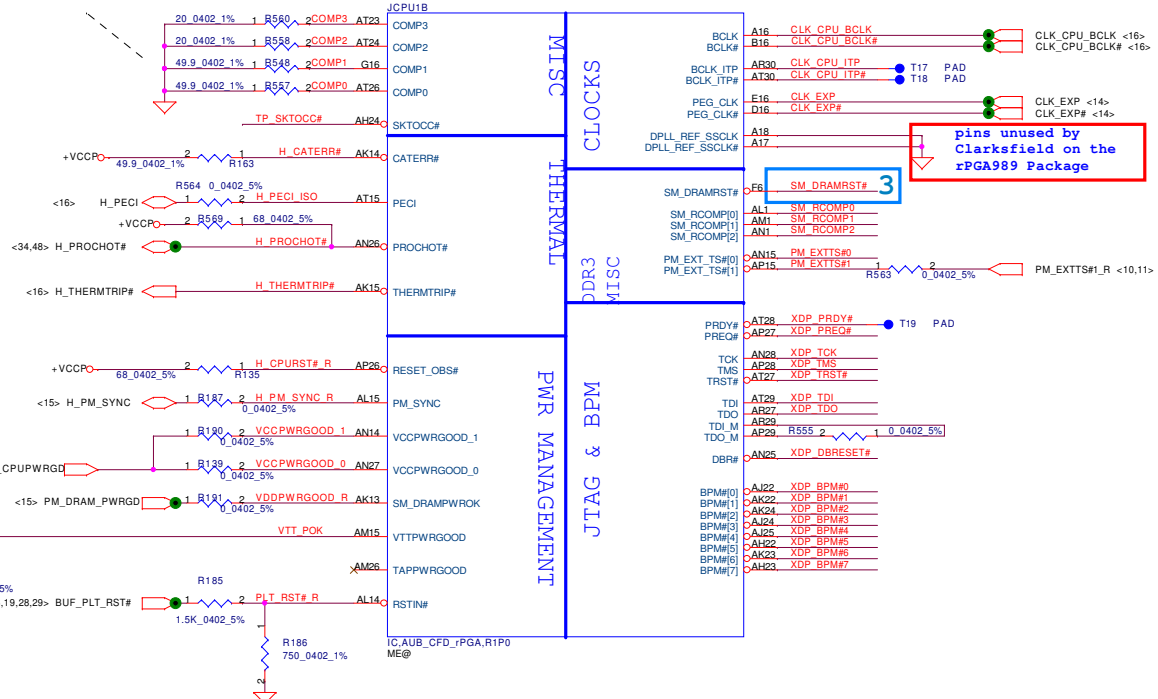
Power Sequence

The ramp time for any rail must be more than 40us

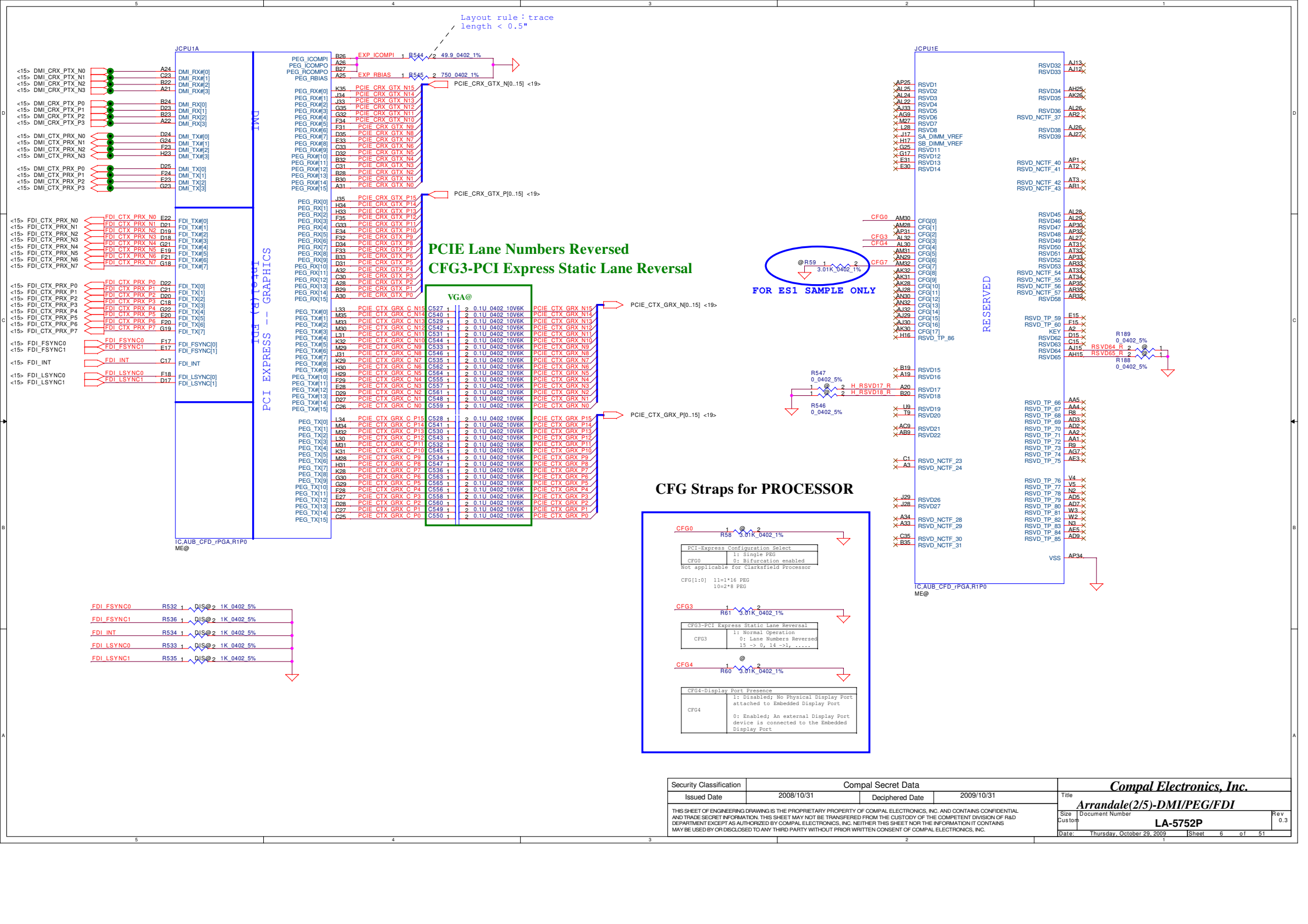


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				VGA Notes List		
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				LA-5752P		
				Date:	Thursday, October 29, 2009	Sheet 4 of 51

Layout rule: 10mil width trace
length < 0.5", spacing 20mil



Security Classification	Compal Secret Data		Title Compal Electronics, Inc. Arrandale(1/5)-Thermal/XDP
Issued Date	2008/10/31	Deciphered Date	
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Date: Thursday, October 29, 2009			Rev 0.3
Sheet 5 of 51			



Layout rule: trace length < 0.5"

**PCIE Lane Numbers Reversed
CFG3-PCI Express Static Lane Reversal**

FOR ES1 SAMPLE ONLY

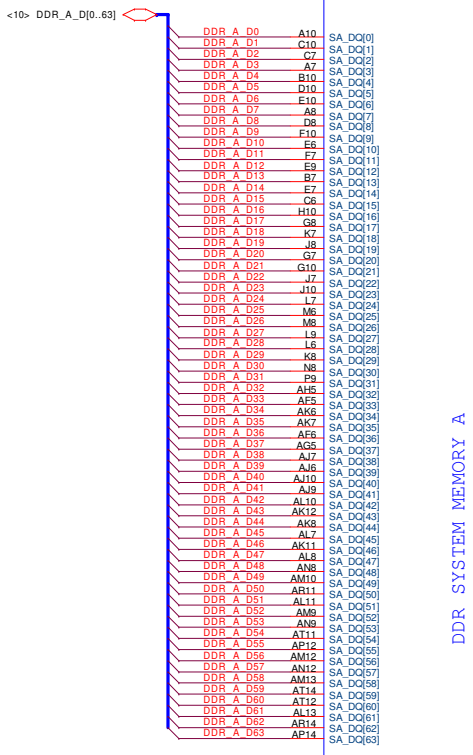
CFG Straps for PROCESSOR

CFG0 PCI-Express Configuration Select CFG0 0: Bifurcation enabled Not applicable for Clarkfield Processor CFG[1:0] 11=1*16 PEG 10=2*8 PEG	
CFG3 CFG3-PCI Express Static Lane Reversal CFG3 1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	
CFG4 CFG4-Display Port Presence 1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port	

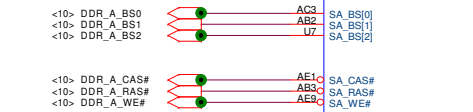
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PEG_ROOMPO	A28						
PEG_RBIAS	B27	EXP RBIAS	R545	2	7.50	0.402	1%
PEG_RX#(0)	K36	PCIE CRX GTX N15					
PEG_RX#(1)	J34	PCIE CRX GTX N14					
PEG_RX#(2)	J33	PCIE CRX GTX N13					
PEG_RX#(3)	G35	PCIE CRX GTX N12					
PEG_RX#(4)	G32	PCIE CRX GTX N11					
PEG_RX#(5)	F34	PCIE CRX GTX N10					
PEG_RX#(6)	F31	PCIE CRX GTX N9					
PEG_RX#(7)	D35	PCIE CRX GTX N8					
PEG_RX#(8)	E33	PCIE CRX GTX N7					
PEG_RX#(9)	C33	PCIE CRX GTX N6					
PEG_RX#(10)	D32	PCIE CRX GTX N5					
PEG_RX#(11)	B32	PCIE CRX GTX N4					
PEG_RX#(12)	C31	PCIE CRX GTX N3					
PEG_RX#(13)	B28	PCIE CRX GTX N2					
PEG_RX#(14)	B30	PCIE CRX GTX N1					
PEG_RX#(15)	A31	PCIE CRX GTX N0					
PEG_RX(0)	J35	PCIE CRX GTX P15					
PEG_RX(1)	H34	PCIE CRX GTX P14					
PEG_RX(2)	J33	PCIE CRX GTX P13					
PEG_RX(3)	F35	PCIE CRX GTX P12					
PEG_RX(4)	G32	PCIE CRX GTX P11					
PEG_RX(5)	F34	PCIE CRX GTX P10					
PEG_RX(6)	F31	PCIE CRX GTX P9					
PEG_RX(7)	D34	PCIE CRX GTX P8					
PEG_RX(8)	E33	PCIE CRX GTX P7					
PEG_RX(9)	D31	PCIE CRX GTX P6					
PEG_RX(10)	A32	PCIE CRX GTX P5					
PEG_RX(11)	C30	PCIE CRX GTX P4					
PEG_RX(12)	A28	PCIE CRX GTX P3					
PEG_RX(13)	B29	PCIE CRX GTX P2					
PEG_RX(14)	A30	PCIE CRX GTX P1					
PEG_RX(15)							
PEG_TX(0)	L33	PCIE CTX GRX C N15	C527	2	0.1U	0.402	10V6K
PEG_TX(1)	M35	PCIE CTX GRX C N13	C540	2	0.1U	0.402	10V6K
PEG_TX(2)	M30	PCIE CTX GRX C N12	C542	2	0.1U	0.402	10V6K
PEG_TX(3)	L31	PCIE CTX GRX C N11	C531	2	0.1U	0.402	10V6K
PEG_TX(4)	K32	PCIE CTX GRX C N10	C544	2	0.1U	0.402	10V6K
PEG_TX(5)	M29	PCIE CTX GRX C N9	C533	2	0.1U	0.402	10V6K
PEG_TX(6)	J31	PCIE CTX GRX C N8	C546	2	0.1U	0.402	10V6K
PEG_TX(7)	K29	PCIE CTX GRX C N7	C535	2	0.1U	0.402	10V6K
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PEG_TX(9)	H29	PCIE CTX GRX C N5	C564	2	0.1U	0.402	10V6K
PEG_TX(10)	E29	PCIE CTX GRX C N4	C555	2	0.1U	0.402	10V6K
PEG_TX(11)	E28	PCIE CTX GRX C N3	C557	2	0.1U	0.402	10V6K
PEG_TX(12)	D29	PCIE CTX GRX C N2	C561	2	0.1U	0.402	10V6K
PEG_TX(13)	D27	PCIE CTX GRX C N1	C548	2	0.1U	0.402	10V6K
PEG_TX(14)	C26	PCIE CTX GRX C N0	C559	2	0.1U	0.402	10V6K
PEG_TX(15)							
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PEG_TX(1)	M34	PCIE CTX GRX C P13	C541	2	0.1U	0.402	10V6K
PEG_TX(2)	L30	PCIE CTX GRX C P12	C543	2	0.1U	0.402	10V6K
PEG_TX(3)	M31	PCIE CTX GRX C P11	C532	2	0.1U	0.402	10V6K
PEG_TX(4)	K31	PCIE CTX GRX C P10	C545	2	0.1U	0.402	10V6K
PEG_TX(5)	M28	PCIE CTX GRX C P9	C534	2	0.1U	0.402	10V6K
PEG_TX(6)	H31	PCIE CTX GRX C P8	C547	2	0.1U	0.402	10V6K
PEG_TX(7)	K28	PCIE CTX GRX C P7	C536	2	0.1U	0.402	10V6K
PEG_TX(8)	G30	PCIE CTX GRX C P6	C563	2	0.1U	0.402	10V6K
PEG_TX(9)	G29	PCIE CTX GRX C P5	C565	2	0.1U	0.402	10V6K
PEG_TX(10)	F29	PCIE CTX GRX C P4	C556	2	0.1U	0.402	10V6K
PEG_TX(11)	E27	PCIE CTX GRX C P3	C558	2	0.1U	0.402	10V6K
PEG_TX(12)	D28	PCIE CTX GRX C P2	C560	2	0.1U	0.402	10V6K
PEG_TX(13)	C27	PCIE CTX GRX C P1	C549	2	0.1U	0.402	10V6K
PEG_TX(14)	C25	PCIE CTX GRX C P0	C550	2	0.1U	0.402	10V6K
PEG_TX(15)							

FDI_FSYNC0	R532	1	DIS@2	1K	0.402	5%
FDI_FSYNC1	R536	1	DIS@2	1K	0.402	5%
FDI_INT	R534	1	DIS@2	1K	0.402	5%
FDI_LSYNC0	R533	1	DIS@2	1K	0.402	5%
FDI_LSYNC1	R535	1	DIS@2	1K	0.402	5%

JCPU1C

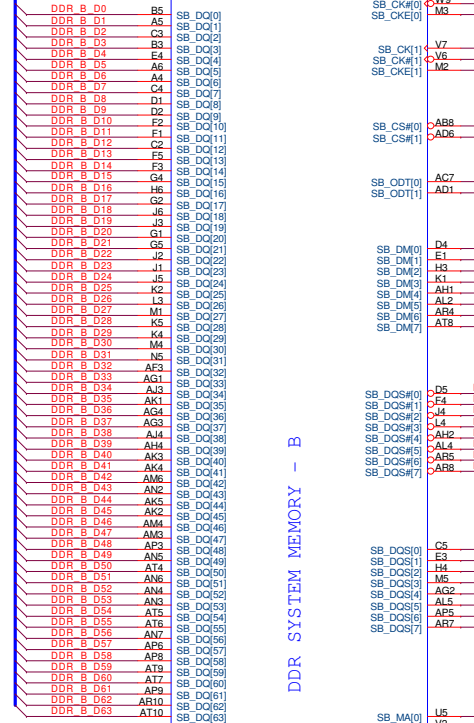


DDR SYSTEM MEMORY A



IC:AUB_CFD_rPGA,R1P0 ME@

JCPU1D

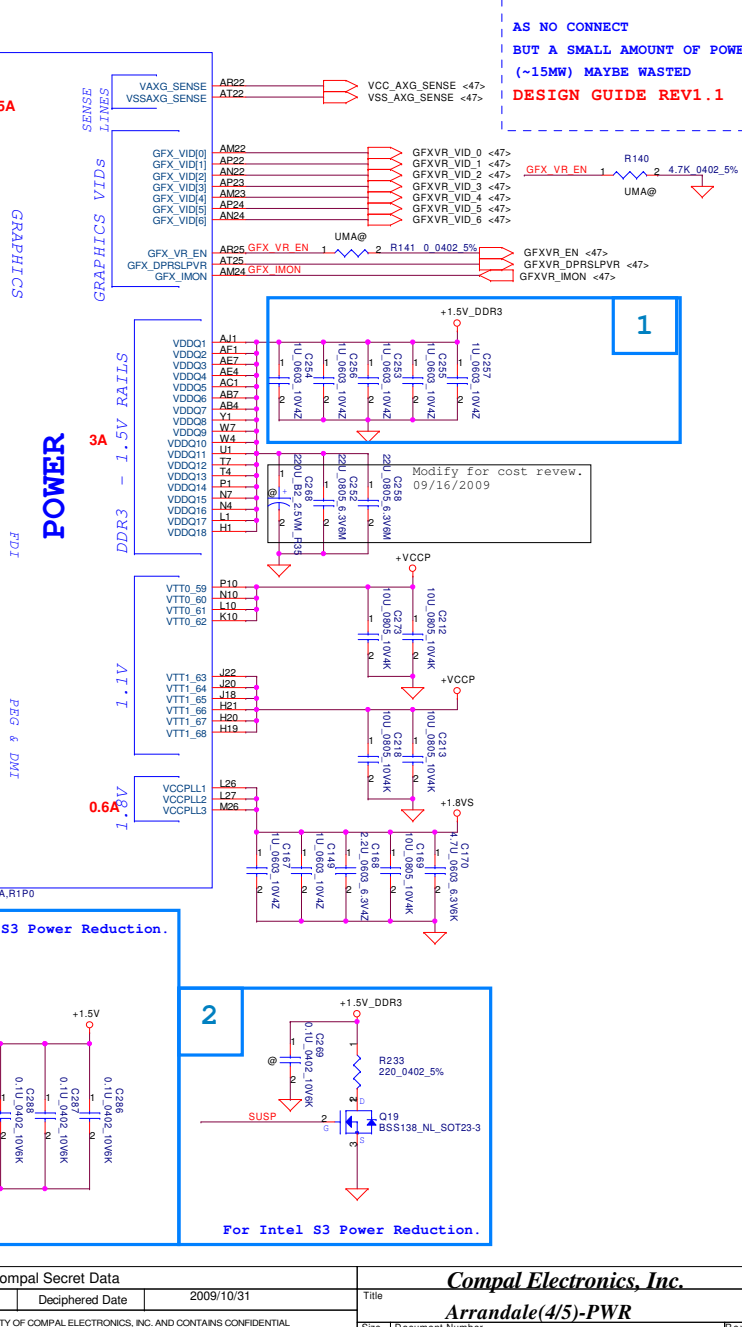
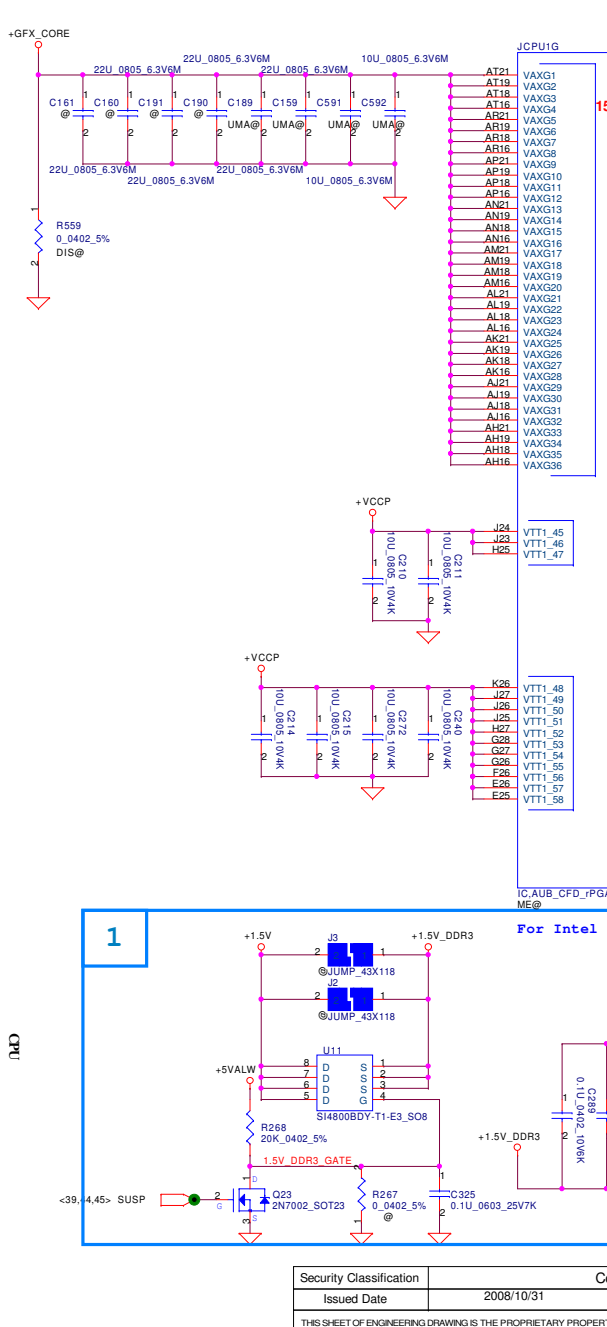
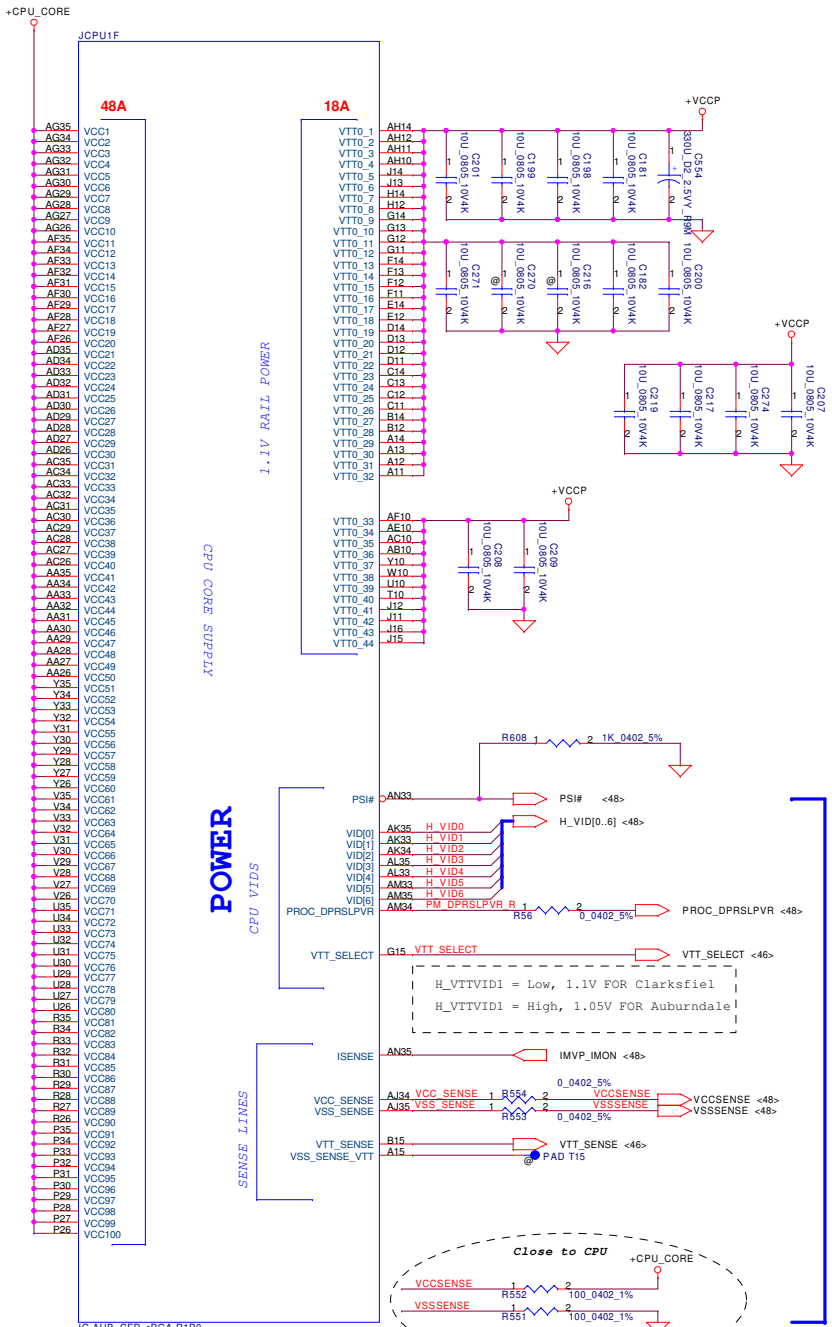


DDR SYSTEM MEMORY - B

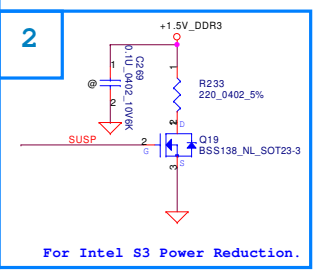
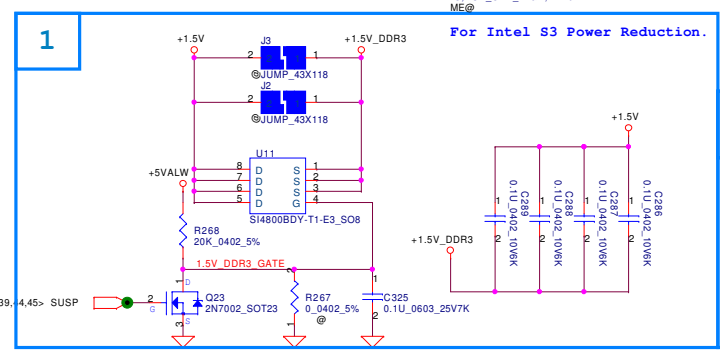
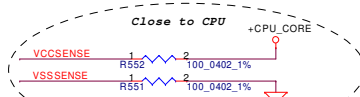


IC:AUB_CFD_rPGA,R1P0 ME@

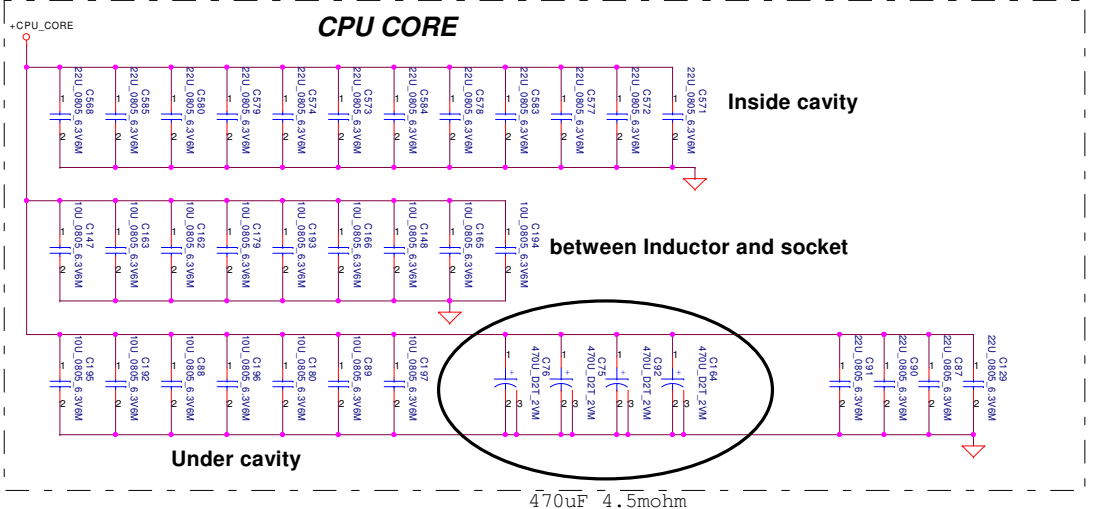
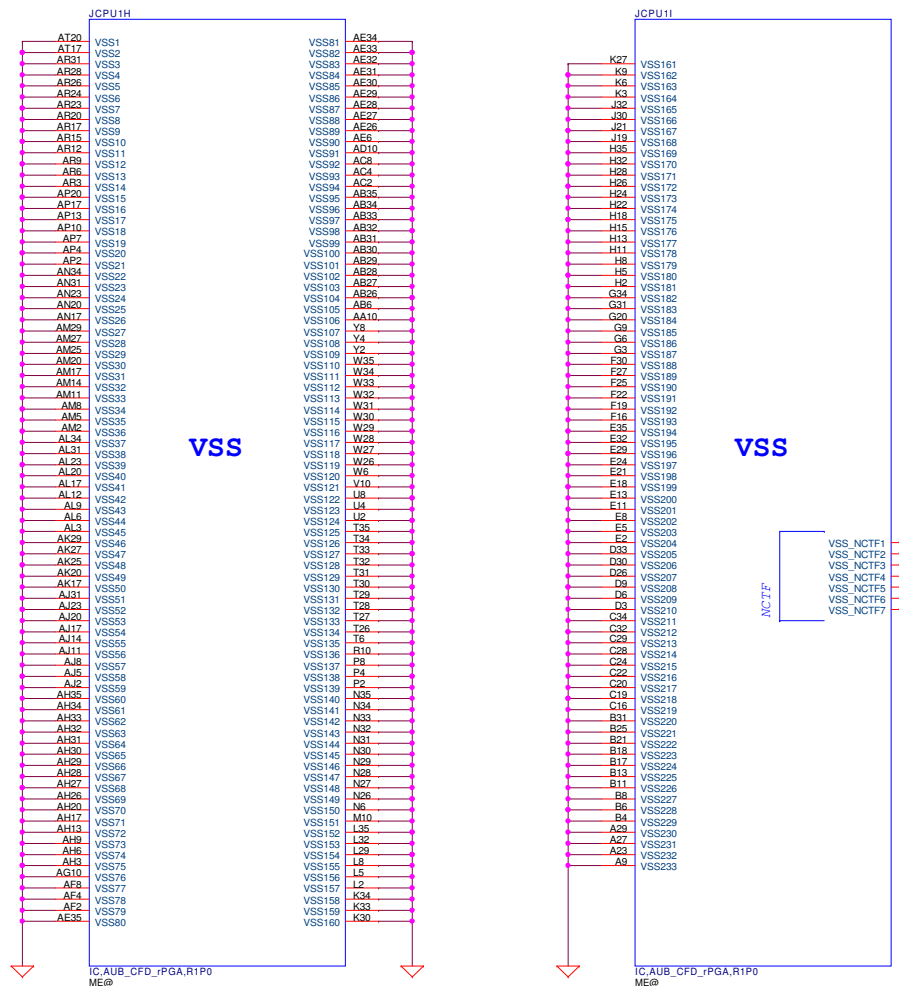
Security Classification	Compal Secret Data		2009/10/31	
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Sub Document Number			Arrandale(3/5)-DDR III	
Rev			0.3	
Date			Thursday, October 29, 2009	
Sheet			7 of 51	



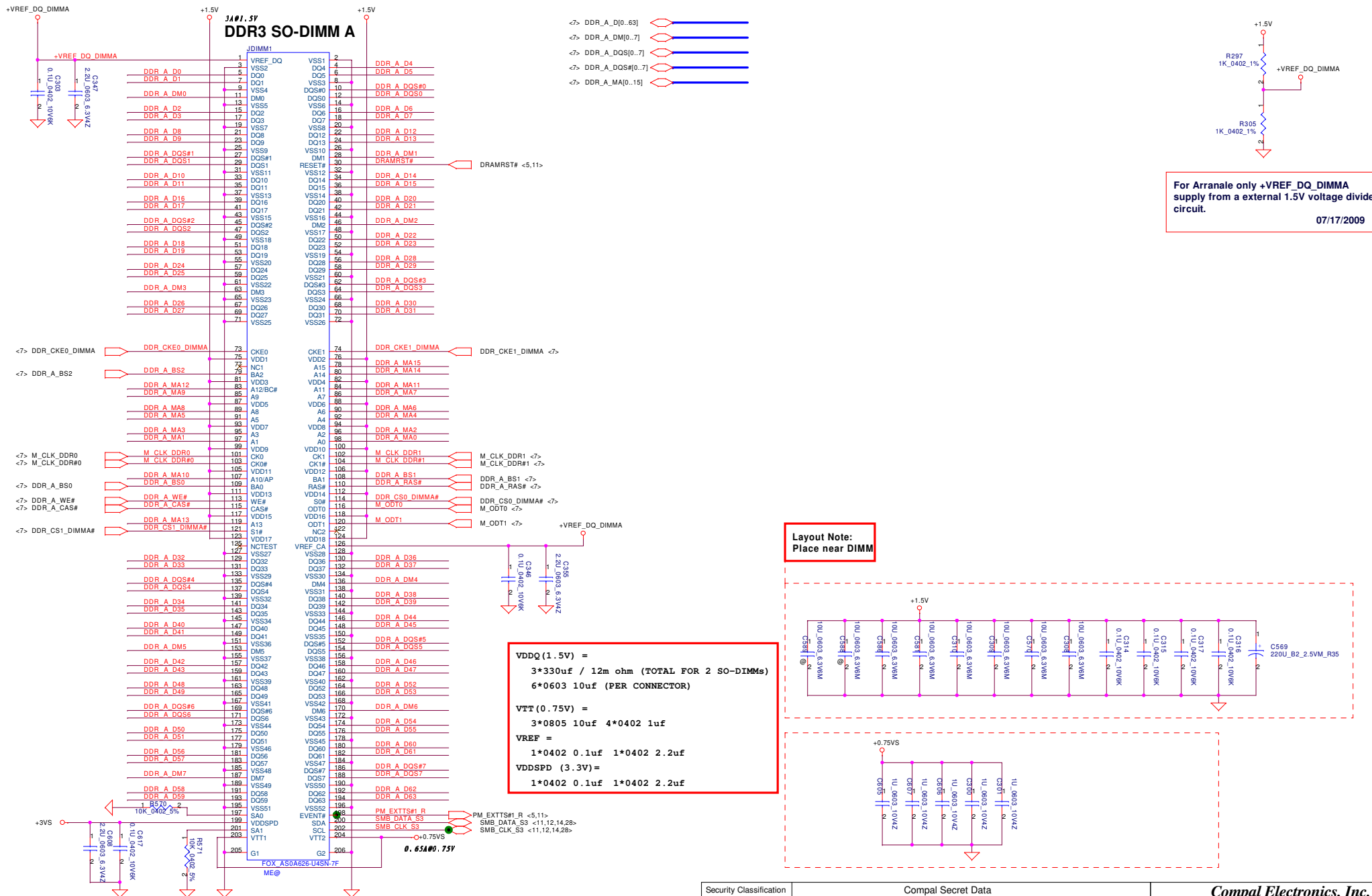
AS NO CONNECT
BUT A SMALL AMOUNT OF POWER
(~15MW) MAYBE WASTED
DESIGN GUIDE REV1.1



Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	Arrandale(4/5)-PWR	
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Customer		0.3			
Date	Thursday, October 29, 2009	Sheet	8	of 51	



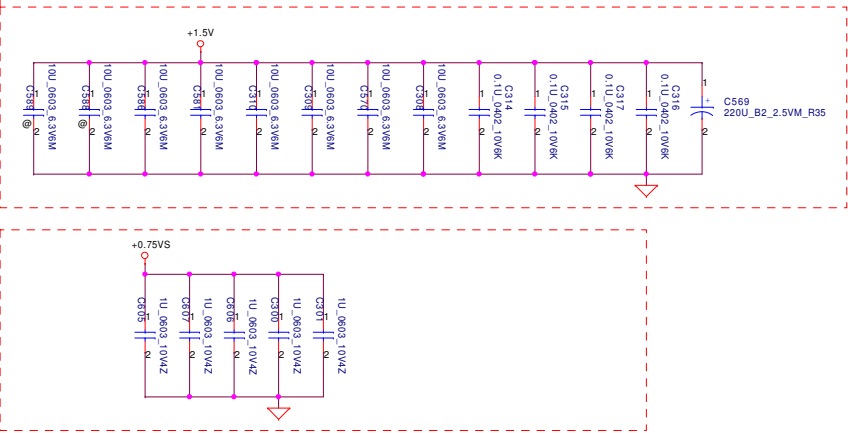
Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	Compal Electronics, Inc.
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For Arranale only +VREF_DQ_DIMMA supply from an external 1.5V voltage divide circuit.

07/17/2009

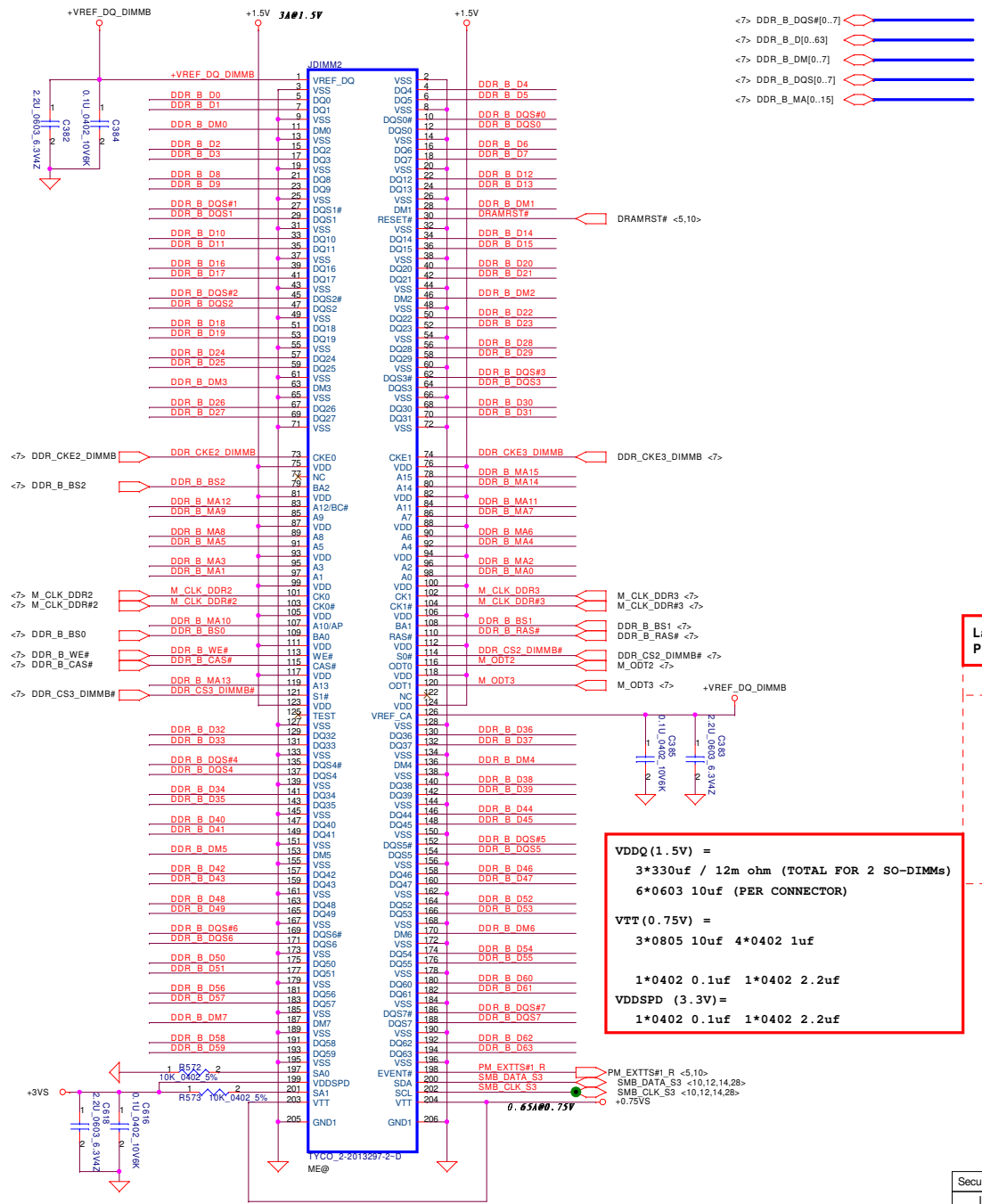
Layout Note:
Place near DIMM



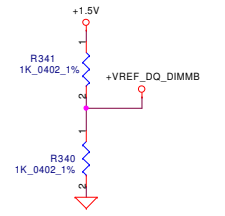
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Issued Date	2008/10/31	Deciphered Date	2009/10/31	Compal Electronics, Inc.	
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				Date	Thursday, October 29, 2009
				Sheet	10 of 51

DDRIII-SODIMM SLOT1

LA-5752P

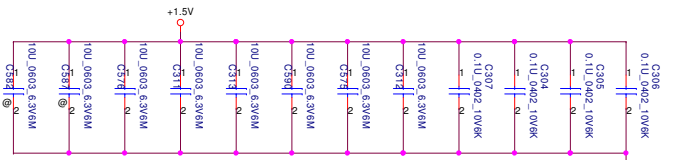


- <7> DDR_B_DQS#0..7
- <7> DDR_B_D0[0..63]
- <7> DDR_B_DM0..7
- <7> DDR_B_DQS0..7
- <7> DDR_B_MA0..15

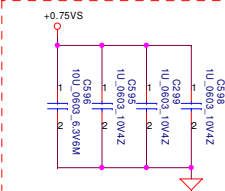


For Arranale only +VREF_DQ_DIMMB supply from an external 1.5V voltage divide circuit.
07/17/2009

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



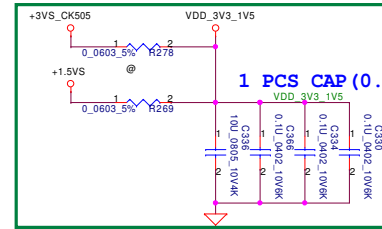
VDDQ (1.5V) =
 $3 \times 330\mu\text{f} / 12\text{m ohm (TOTAL FOR 2 SO-DIMMS)}$
 $6 \times 0603 10\mu\text{f (PER CONNECTOR)}$

VTT (0.75V) =
 $3 \times 0805 10\mu\text{f} 4 \times 0402 1\mu\text{f}$

VDDSPD (3.3V) =
 $1 \times 0402 0.1\mu\text{f} 1 \times 0402 2.2\mu\text{f}$
 $1 \times 0402 0.1\mu\text{f} 1 \times 0402 2.2\mu\text{f}$

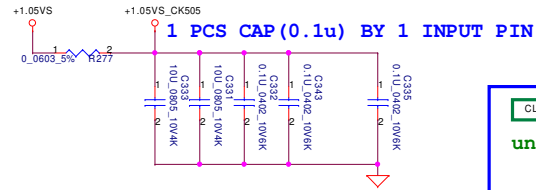
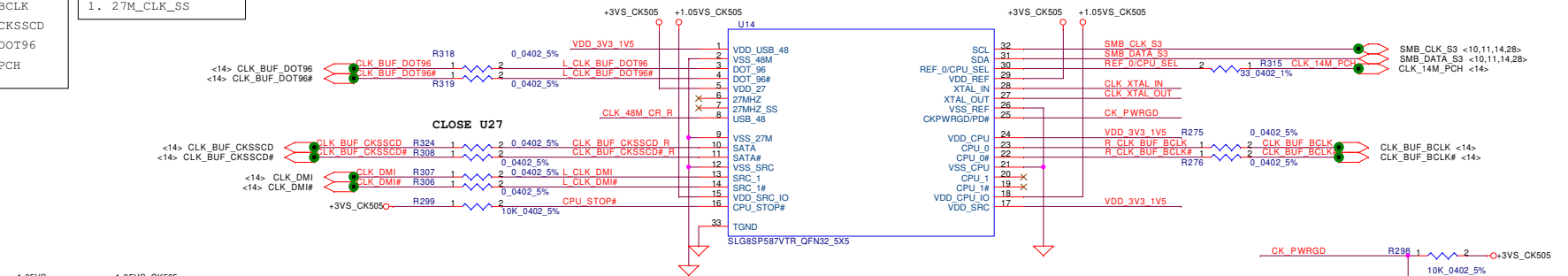
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Issued Date	2008/10/31	Deciphered Date	2009/10/31	2008/10/31
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Document Number			Rev	
LA-5752P			0.3	
Date:	Thursday, October 29, 2009	Sheet	11	of 51

Reserve for Low Power CLK GEN.
 RTM890N-632
 SLG8LV597VTR

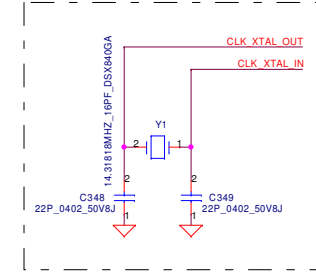
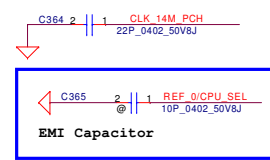
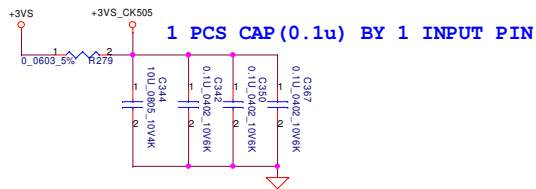
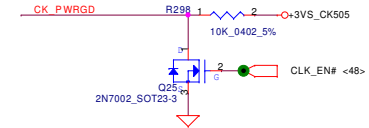
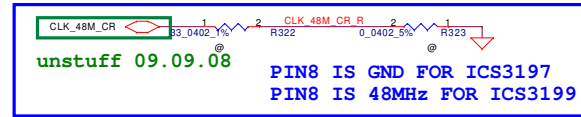


- CLK GEN TO PCH**
1. CLK_DMI
 2. CLK_BUF_BCLK
 3. CLK_BUF_CKSSCD
 4. CLK_BUF_DOT96
 5. CLK_14M_PCH

- CLK GEN TO VGA**
1. 27M_CLK
 1. 27M_CLK_SS

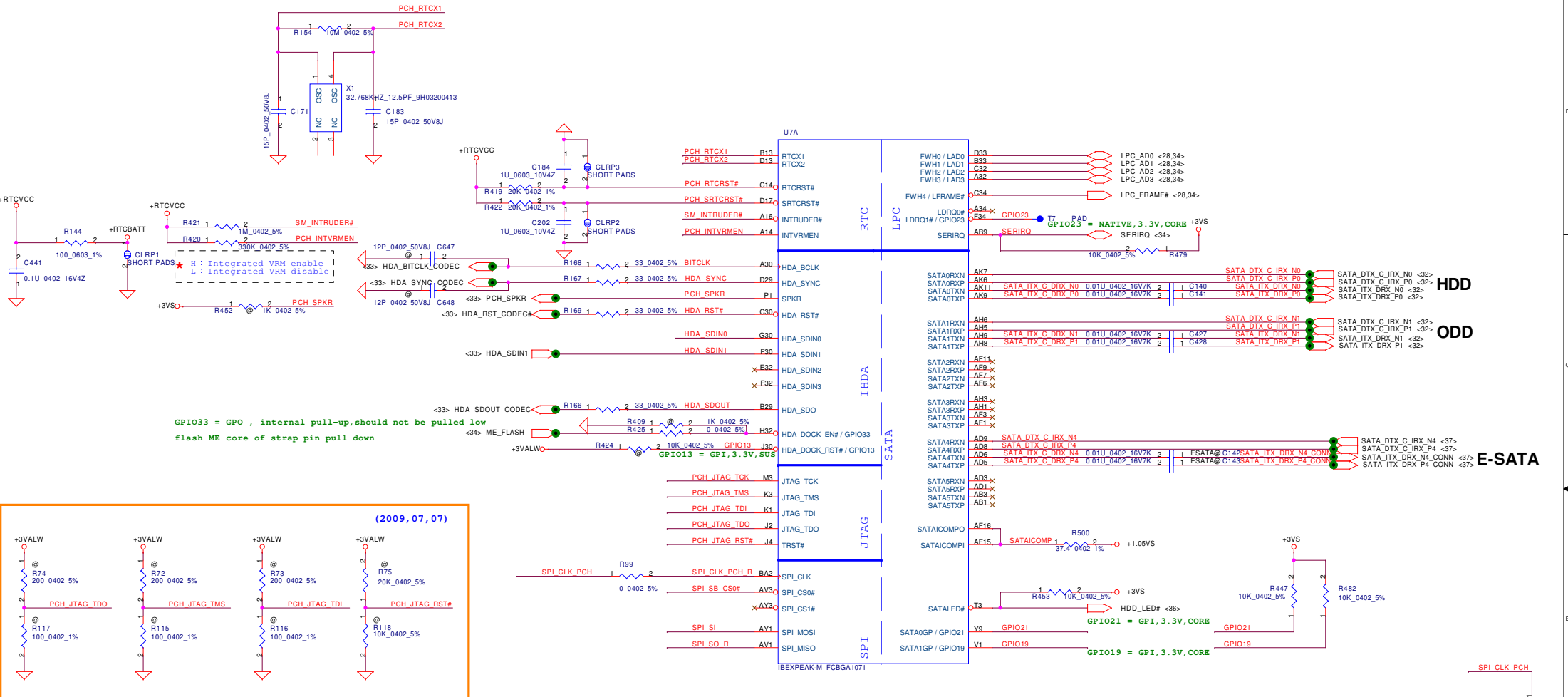


RTM890N-631-GRT QFN 32P CLK GEN (SA00003HQ00)
 ICS9LV5319AKLF T MLF 32P CLK GEN (SA00003HR00)

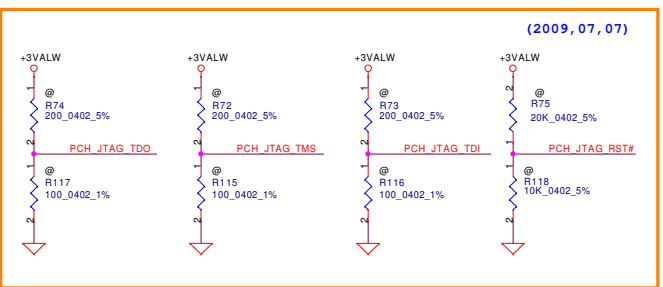


PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	CLOCK GENERATOR
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Size				Document Number
				LA-5752P
Date:				Thursday, October 29, 2009
				Sheet 12 of 51

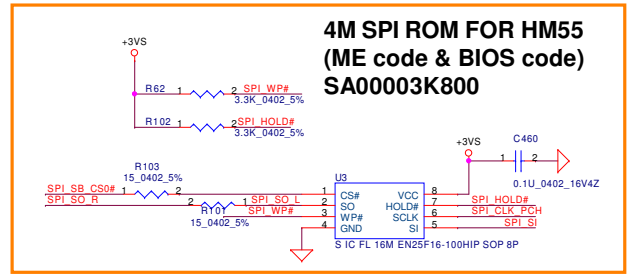


GPIO33 = GPO , internal pull-up, should not be pulled low
flash ME core of strap pin pull down



PCH_JTAG TCK R114 1 2 51 0402 5% (2009, 05, 04)
FOR INTEL DPDG REV1.6 (MAY 2009)

PCH Pin	RefDes	PCH JTAG Pre-Production		PCH JTAG Production
		ES1	ES2	★ MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
	R590	No Install	100ohm	No Install
PCH_JTAG_TMS	R584	200ohm	200ohm	No Install
	R583	100ohm	100ohm	No Install
PCH_JTAG_TDI	R587	200ohm	200ohm	No Install
	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
	R595	20Kohm	20Kohm	No Install
PCH_JTAG_RST#	R594	10Kohm	10Kohm	No Install



Security Classification	Compal Secret Data		Title IBEX-M(1/6)-HDA/JTAG/SATA
Issued Date	2008/10/31	Deciphered Date	

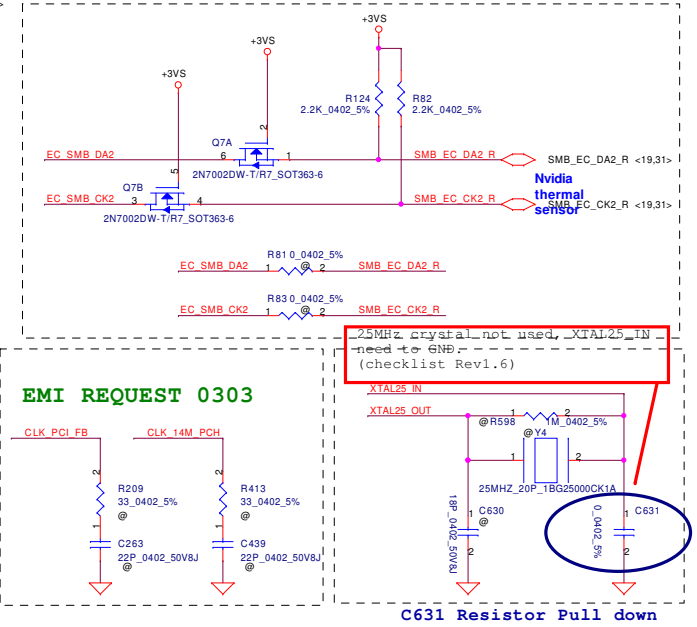
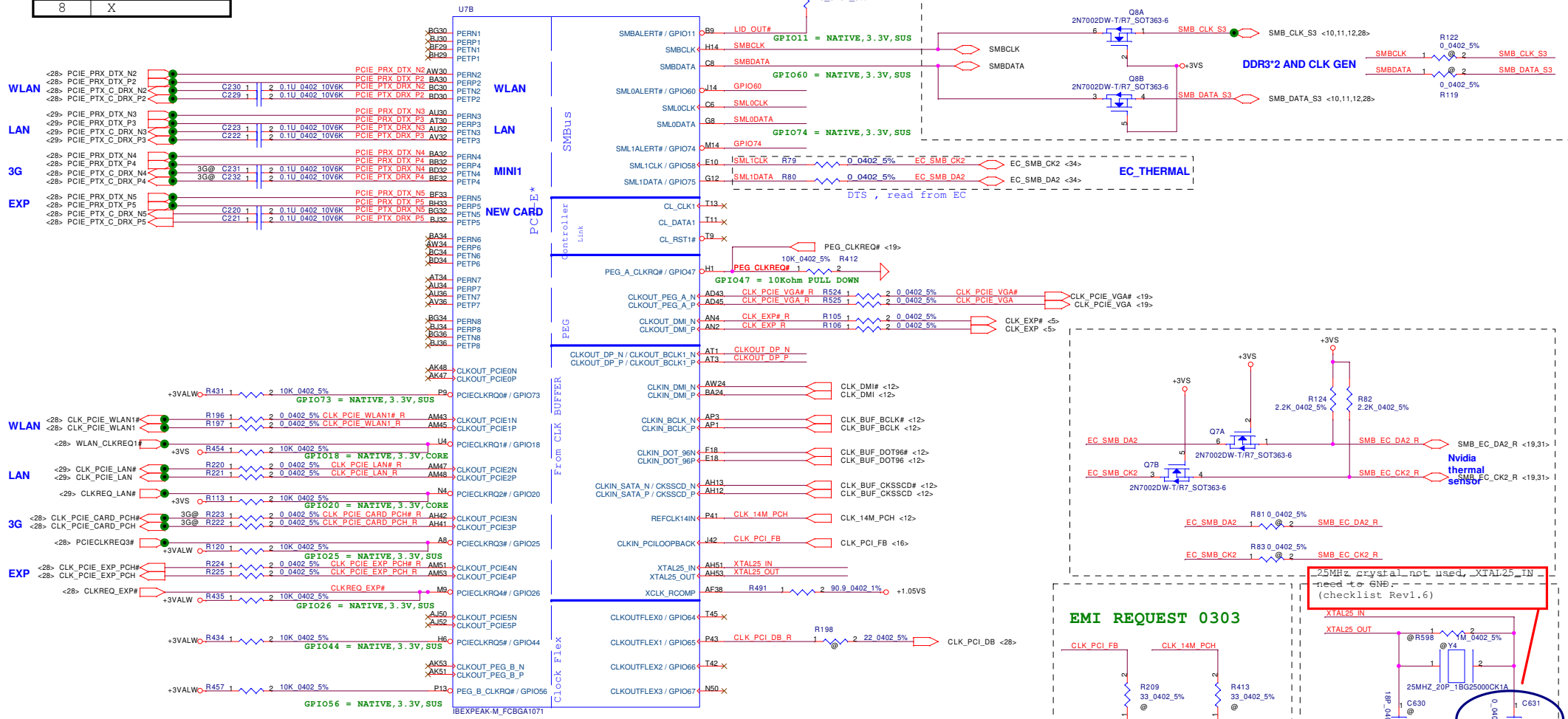
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Site	Document Number	Rev
Customer	LA-5752P	0.3

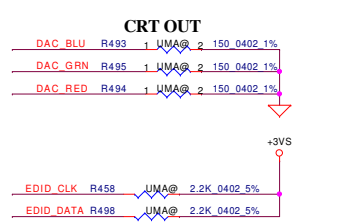
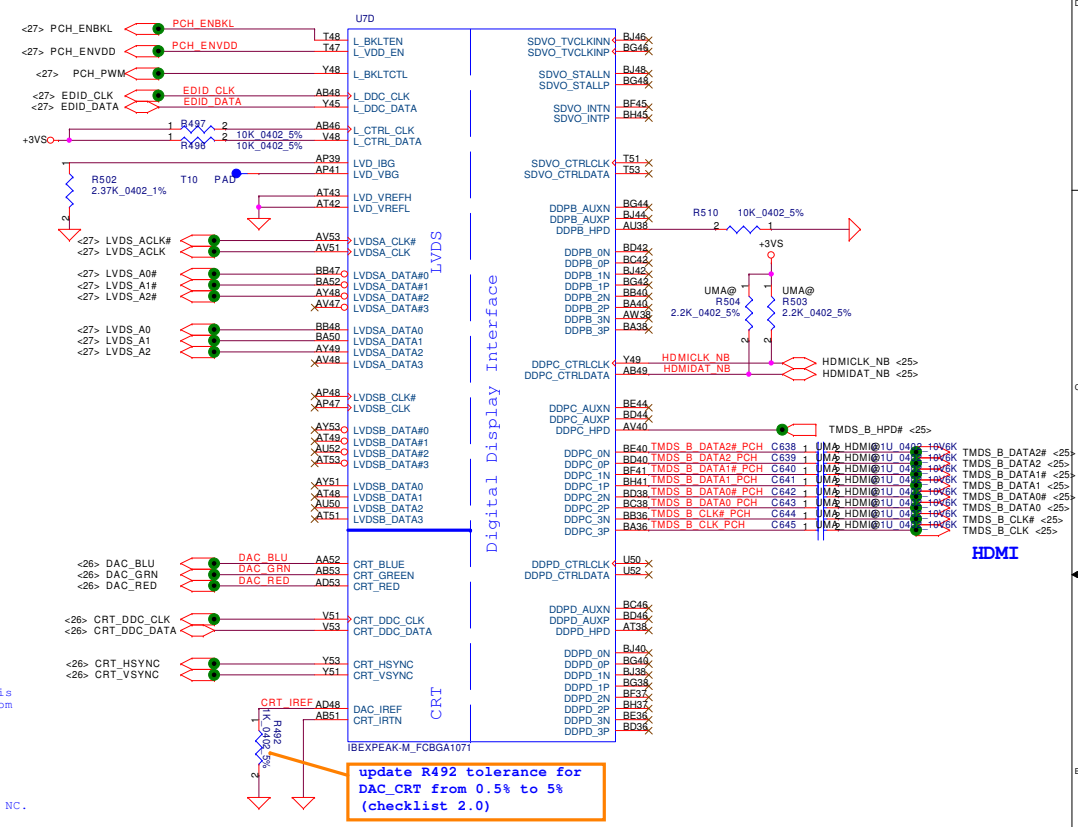
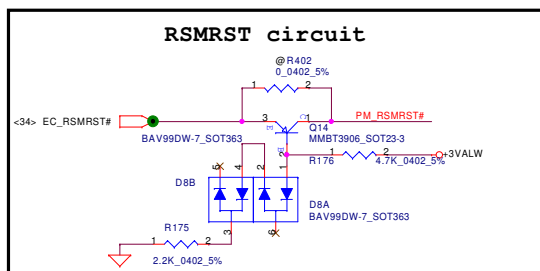
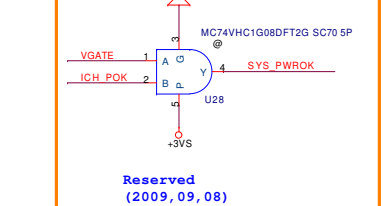
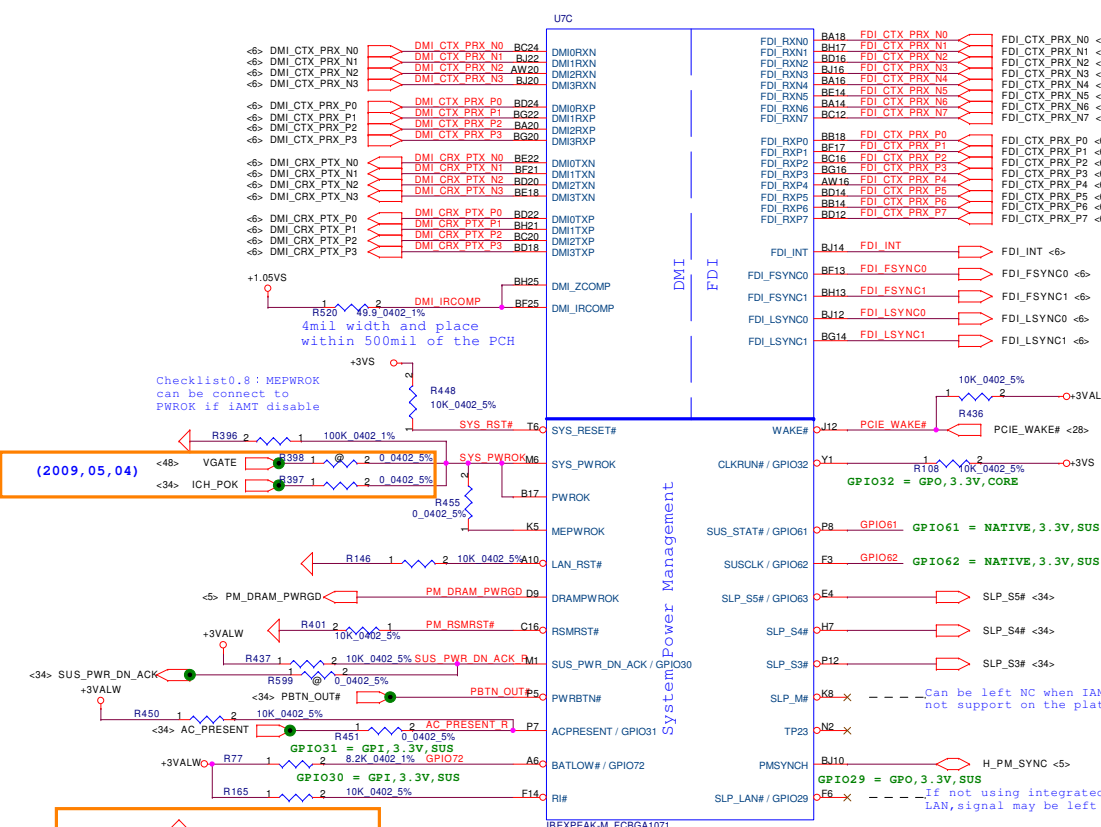
Date: Thursday, October 29, 2009 | Sheet 13 of 51

PCI-E PORT LIST

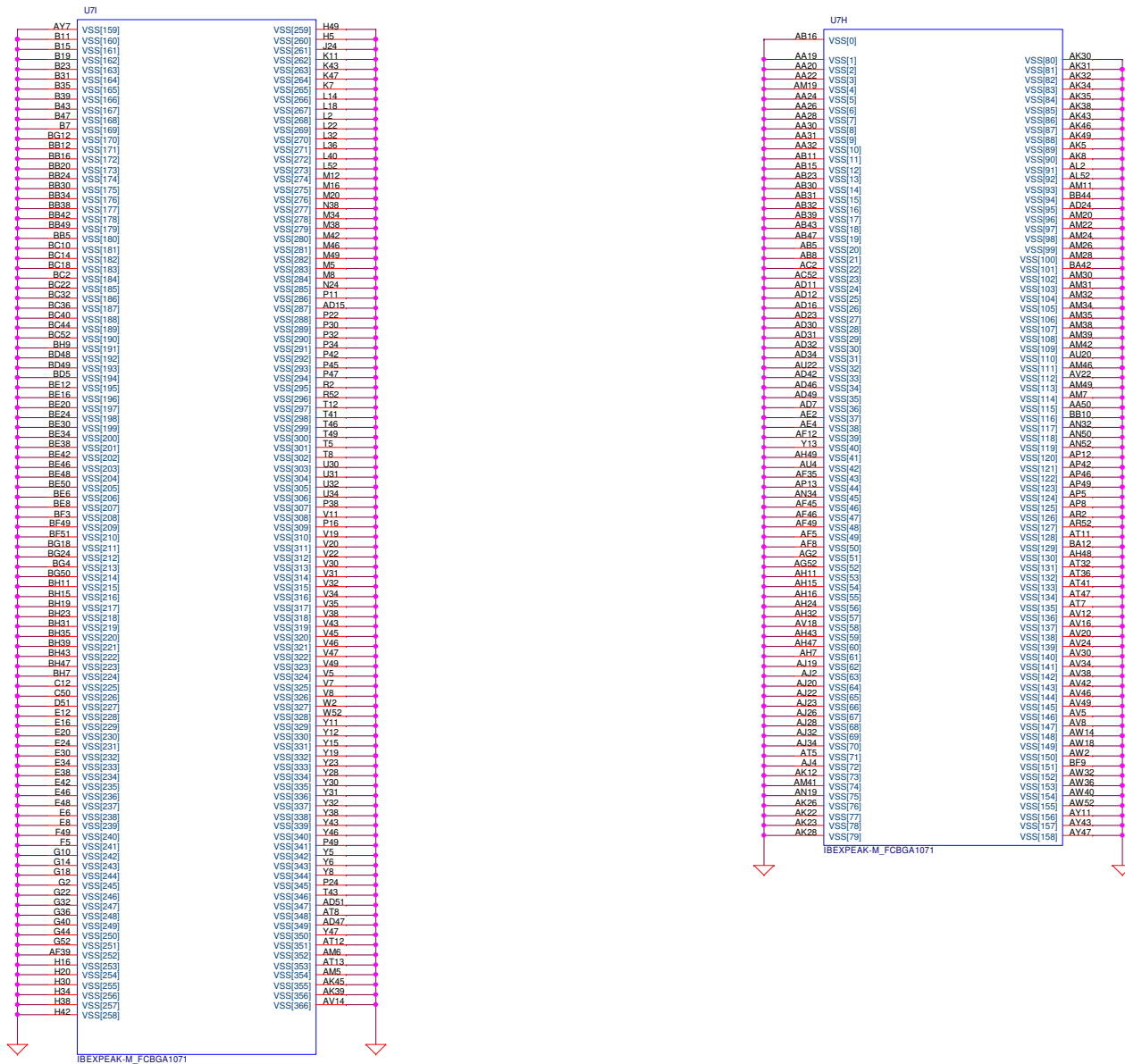
PORT	DEVICE
1	X
2	WLAN
3	LAN
4	3G
5	NEW CARD
6	X
7	X
8	X



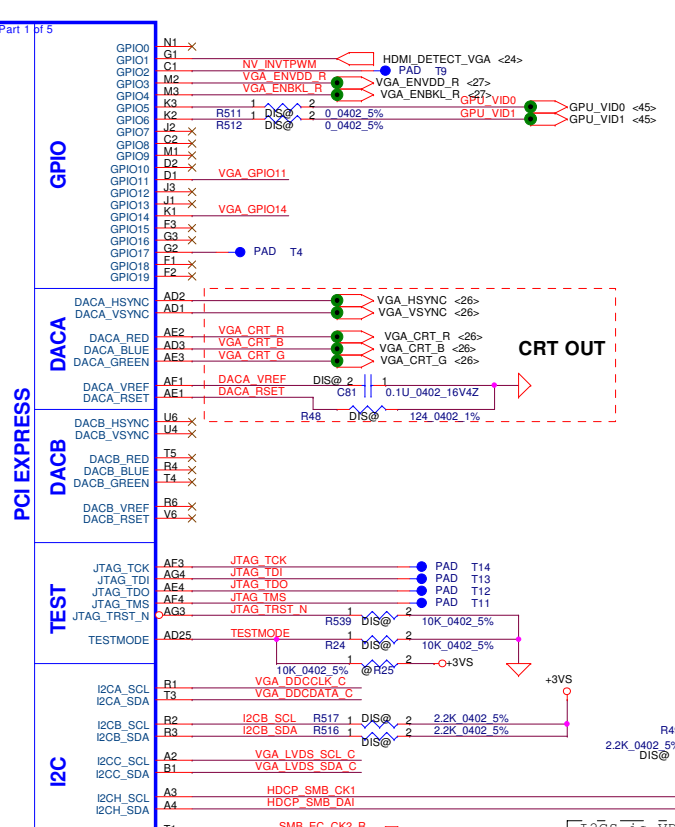
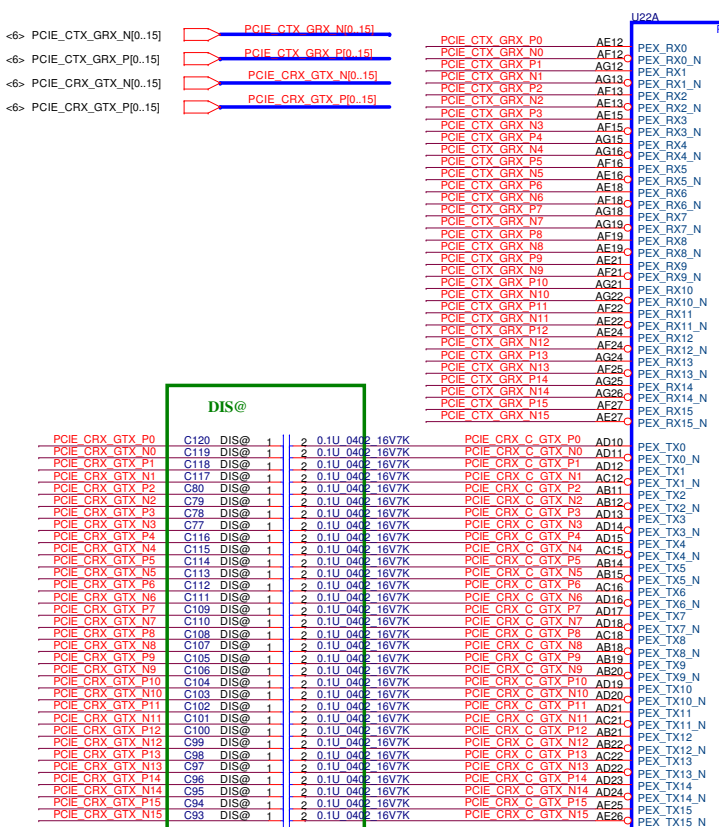
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	1 IBEX-M(2/6)-PCI-E/SMBUS/CLK	
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			Custom	LA-5752P	0.3
Date:	Thursday, October 29, 2009	Sheet	14	of	51



Security Classification	Compal Secret Data		Title	
Issued Date	2008/10/31	Deciphered Date	2009/10/31	IBEX-M(3/6)-DMI/GPIO/LVDS
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S329	Document Number	LA-5752P		Rev 0.3
Date:	Thursday, October 29, 2009	Sheet	15	of 51



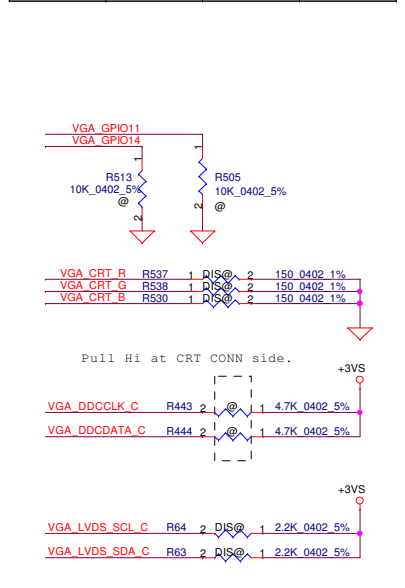
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Issued Date	2008/10/31	Deciphered Date	
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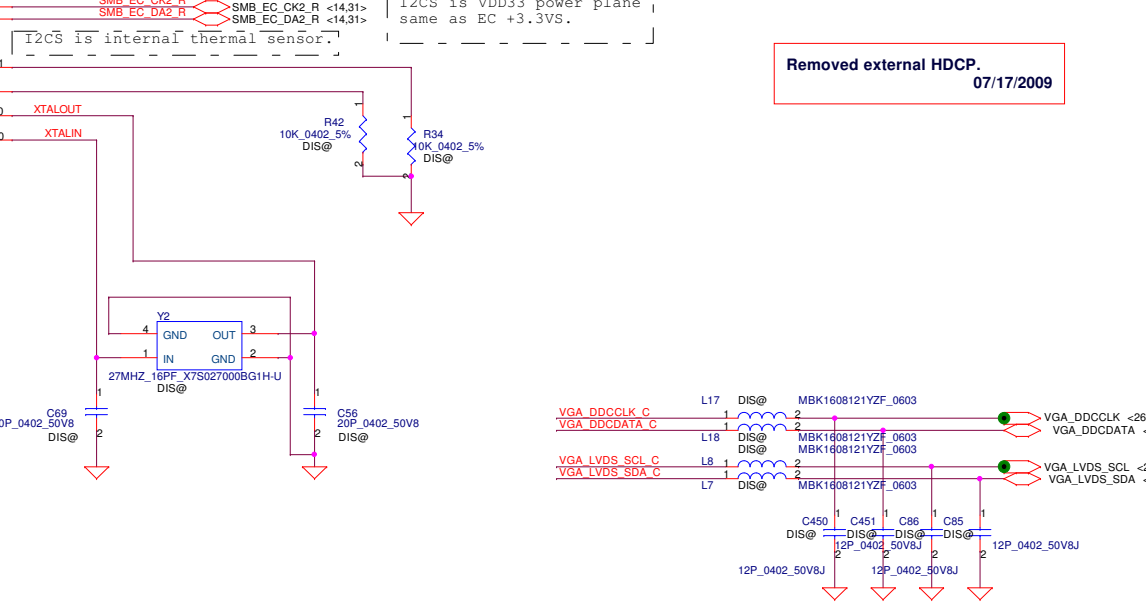
Device ID	Device ID
N10M-GS (40nm)	0x0A74
N11M-GE1/LP1 (40nm)	0x0A7D

GPIO5 GPU_VID0	GPIO6 GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	1.0V	P0

GPIO5 GPU_VID0	GPIO6 GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	0.9V	P0



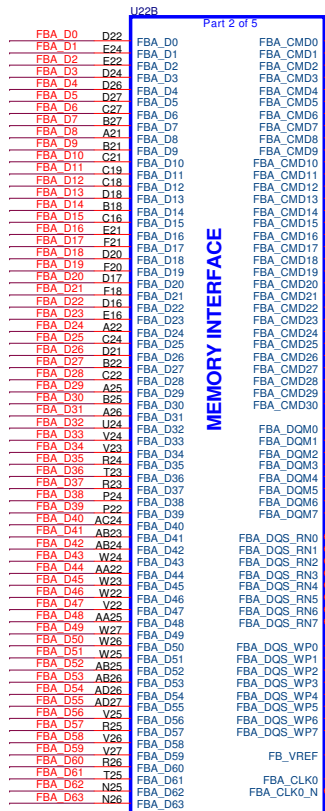
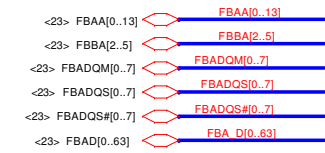
Removed external HDCP. 07/17/2009



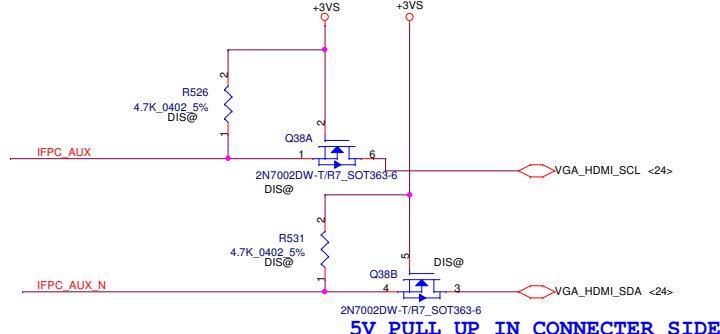
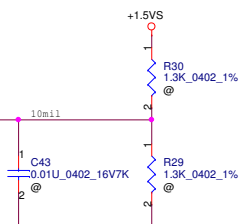
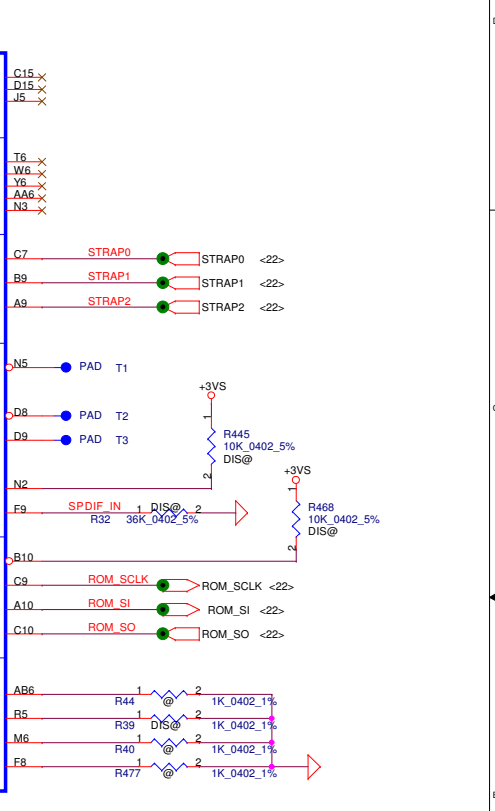
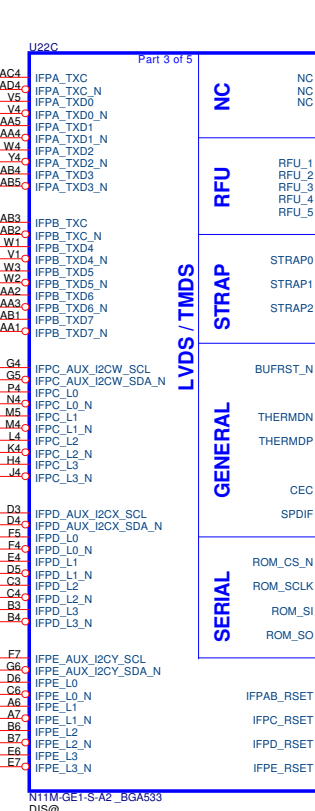
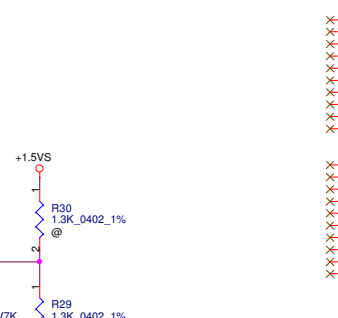
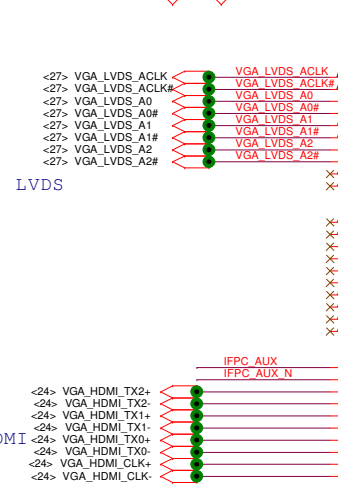
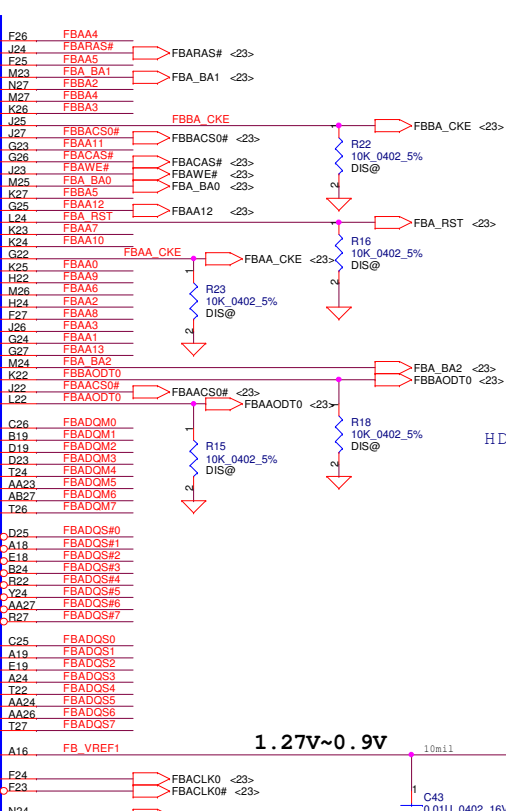
Security Classification	Compal Secret Data	
Issued Date	2007/10/15	Deciphered Date
		2008/10/15

Compal Electronics, Inc.			
Title			
N10M-GE1 PCIE,GPIO,CLK			
Size	Document Number	Rev	
B	LA-5752P	0.3	
Date:	Thursday, October 29, 2009	Sheet	19 of 51

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MEMORY INTERFACE



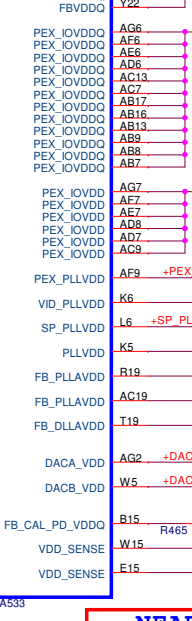
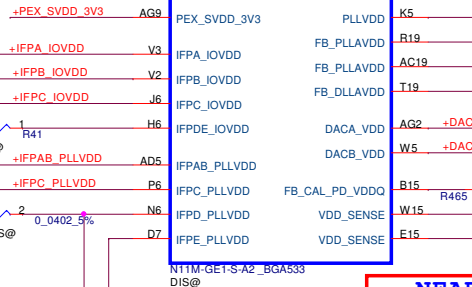
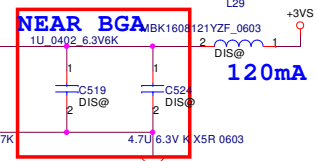
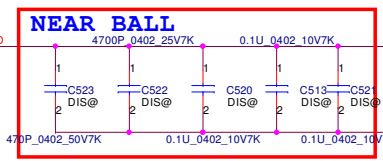
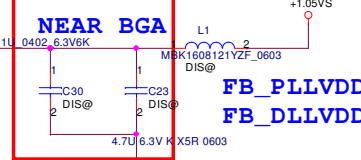
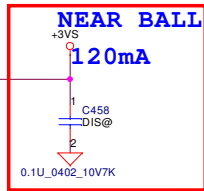
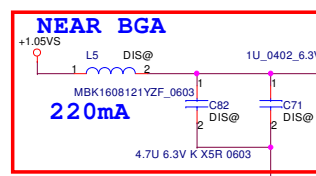
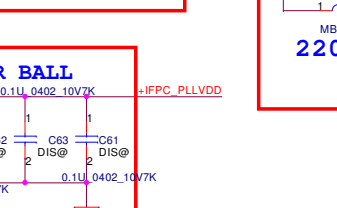
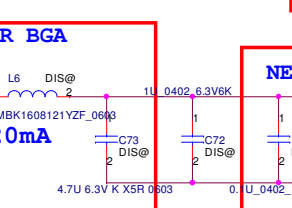
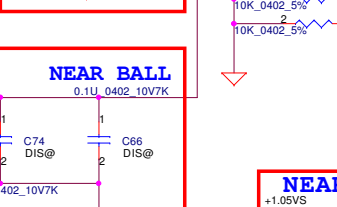
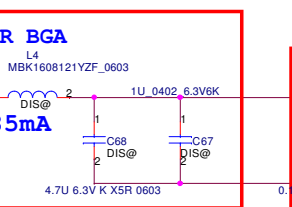
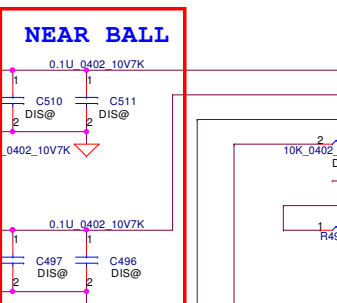
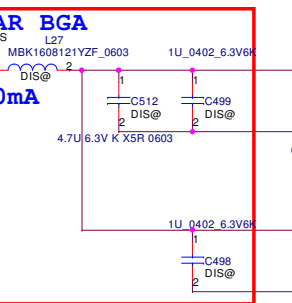
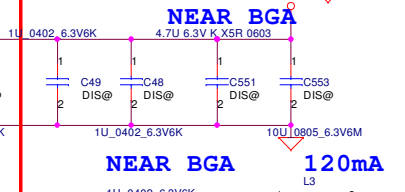
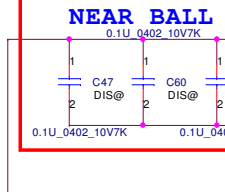
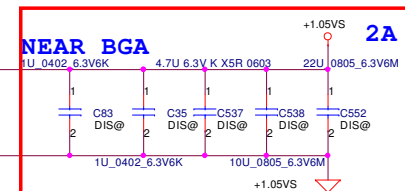
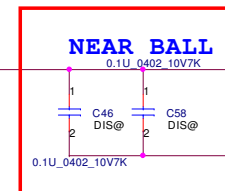
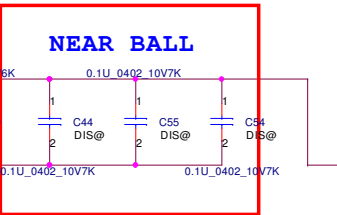
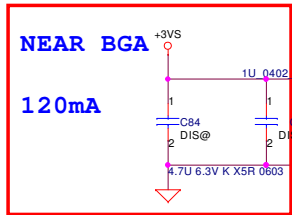
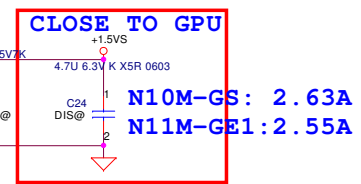
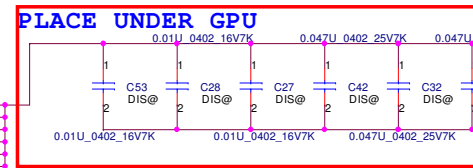
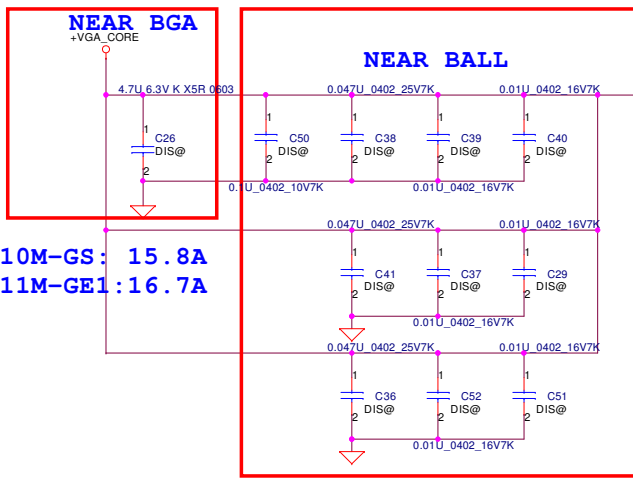
5V PULL UP IN CONNECTER SIDE

Security Classification	Compal Secret Data		Title	
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Date: Thursday, October 29, 2009				Sheet 20 of 51

Compal Electronics, Inc.

N10M-GE1 LVDS, Memory Bus

Size B Document Number LA-5752P Rev 0.3

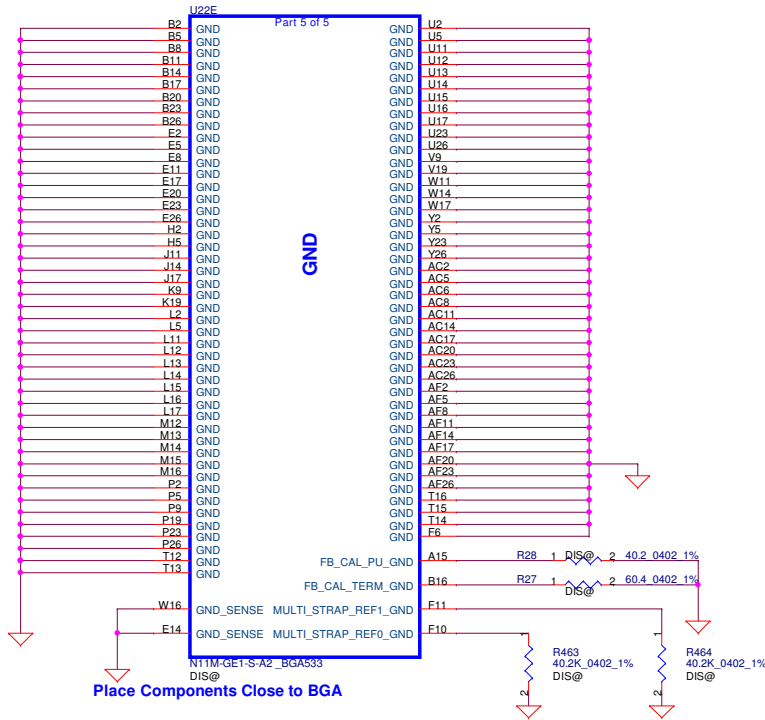


VID_PLLVDD=45mA
SP_PLLVDD=45mA
PLLVDD=60mA

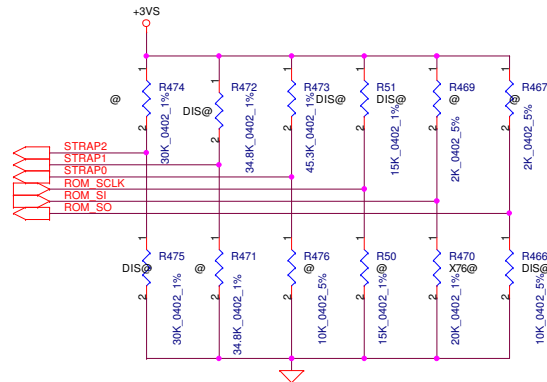
FB_PLLVDD=100mA
FB_DLLVDD=100mA

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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.	
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Size	Document Number	Rev		Date	
Custom	LA-5752P	F.03		Thursday, October 29, 2009	
Sheet		of		Page	
21		51		1	

A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



<20> STRAP2
 <20> STRAP1
 <20> STRAP0
 <20> ROM_SCLK
 <20> ROM_SI
 <20> ROM_SO



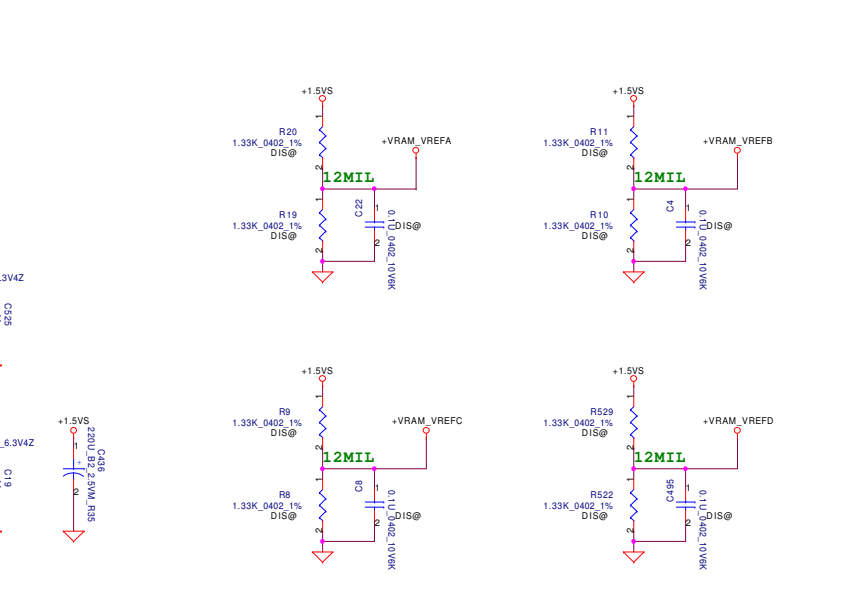
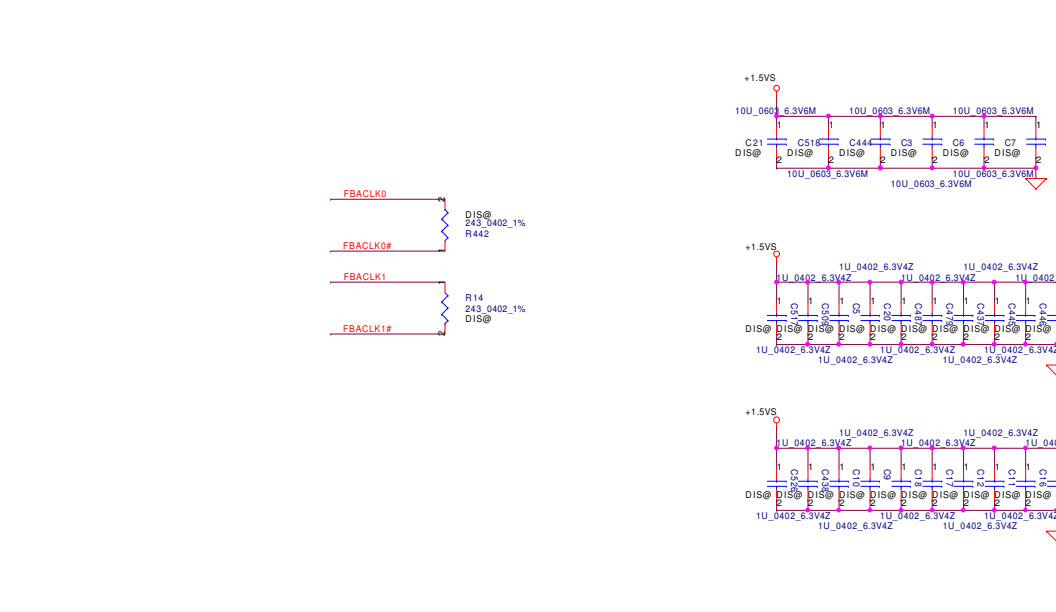
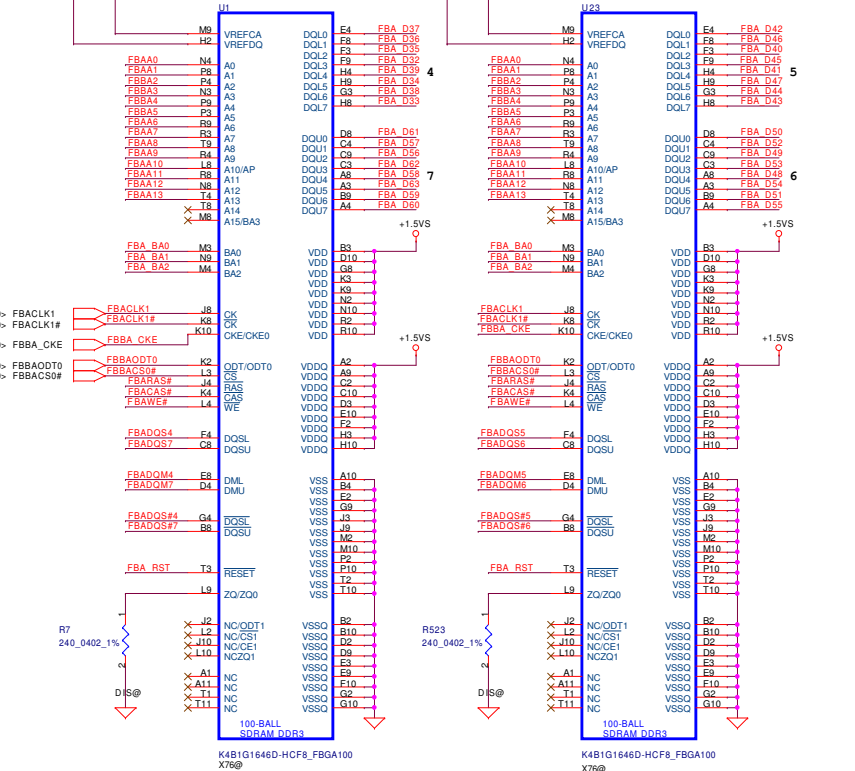
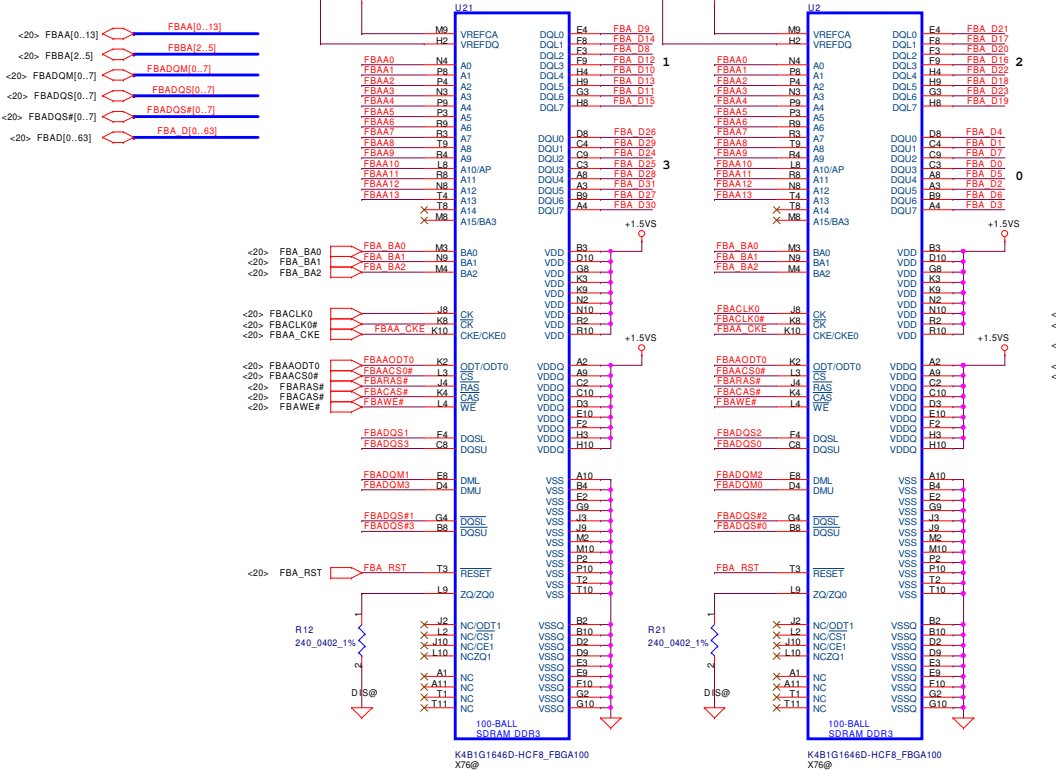
STRAP1 use for 3GIO_PADCFG to set 35K pull up.
 (PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (default)	K4W1G1646E-HC12					
	64Mx16	PD 10K	PD 15K	PD 20K	PU 30K	PU 35K	PU 45K
Hynix 800MHz	H5TQ1G63BFR-12C						
	64Mx16	PD 10K	PD 15K	PD 15K	PU 30K	PU 35K	PU 45K
				X76			

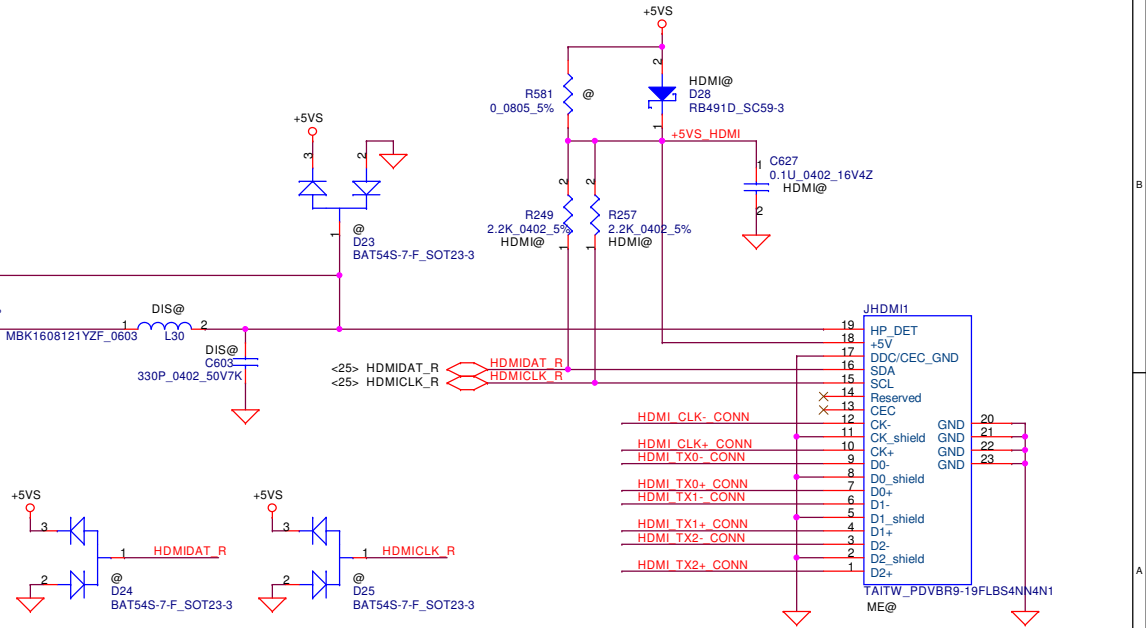
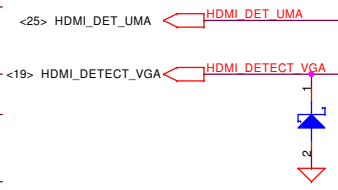
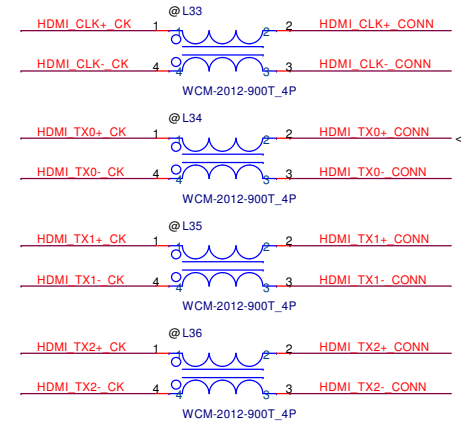
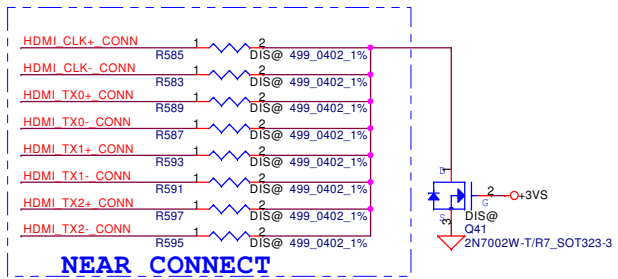
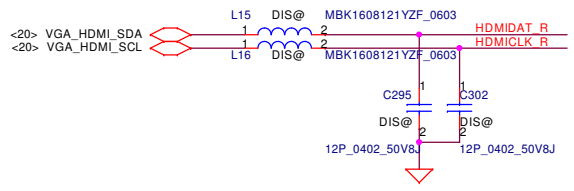
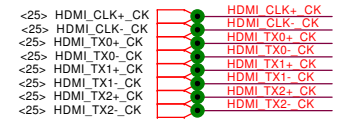
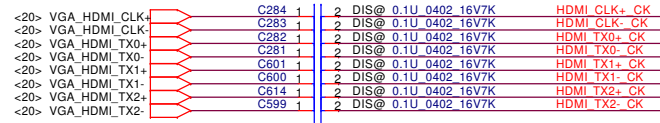
N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resistor for driver calibration DG-04642-001-V01(May 22, 2009)

N10x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001



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Size	Document Number	Rev		
	LA-5752P	0.3		
Date:	Thursday, October 29, 2009	Sheet	23	of 51



HDMI_CLK+_CK	R584	1	HDMI@	2	0	0402	5%	HDMI_CLK+_CONN
HDMI_CLK-_CK	R582	1	HDMI@	2	0	0402	5%	HDMI_CLK-_CONN
HDMI_TX0+_CK	R588	1	HDMI@	2	0	0402	5%	HDMI_TX0+_CONN
HDMI_TX0-_CK	R586	1	HDMI@	2	0	0402	5%	HDMI_TX0-_CONN
HDMI_TX1+_CK	R592	1	HDMI@	2	0	0402	5%	HDMI_TX1+_CONN
HDMI_TX1-_CK	R590	1	HDMI@	2	0	0402	5%	HDMI_TX1-_CONN
HDMI_TX2+_CK	R596	1	HDMI@	2	0	0402	5%	HDMI_TX2+_CONN
HDMI_TX2-_CK	R594	1	HDMI@	2	0	0402	5%	HDMI_TX2-_CONN

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Issued Date	2008/03/25	Deciphered Date	2008/04/
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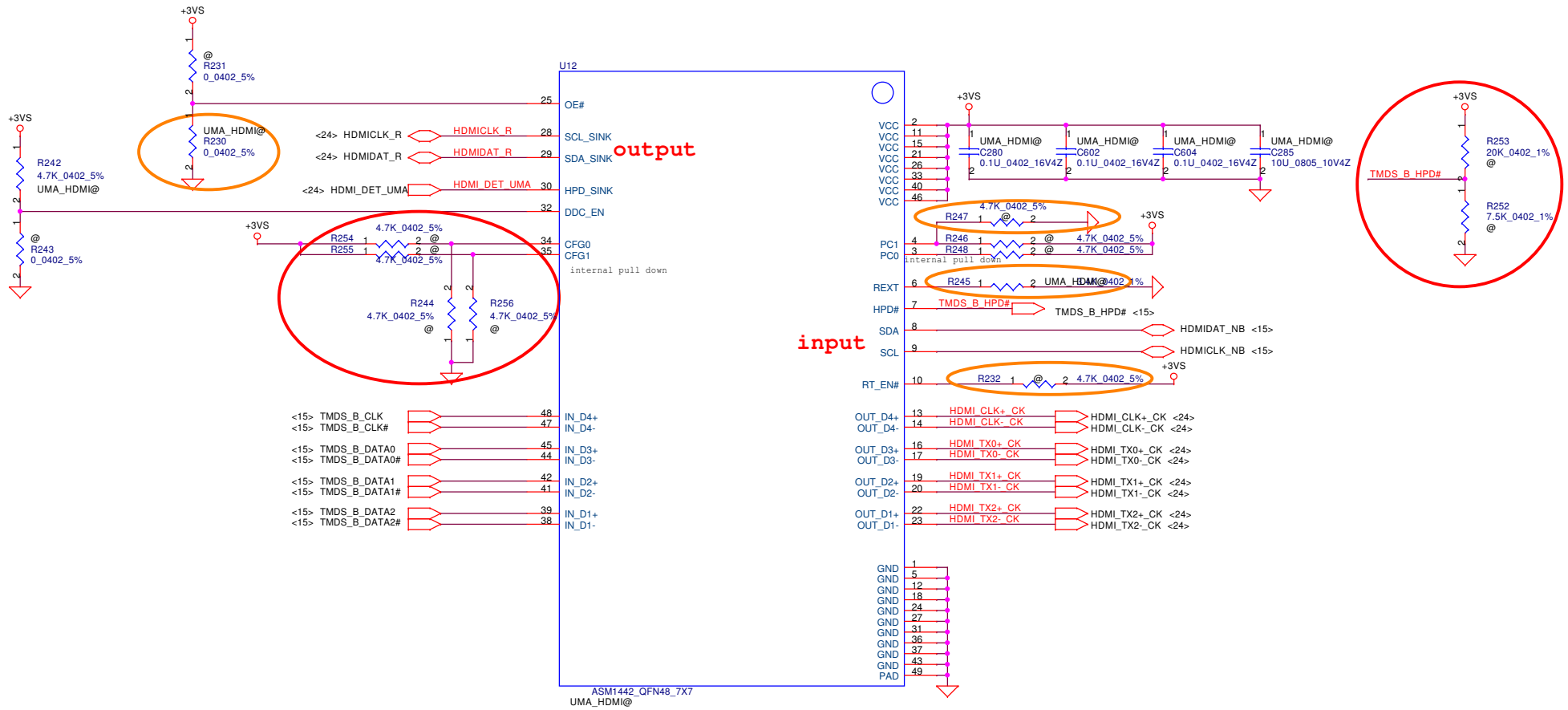
Compal Electronics, Ltd.			
Title			
HDMI CONN			
Size	Document Number	Rev	
Custom	LA-5752P	0.3	
Date:	Thursday, October 29, 2009	Sheet	24 of 51

P/N:SA00003GT00 (ASM1442)

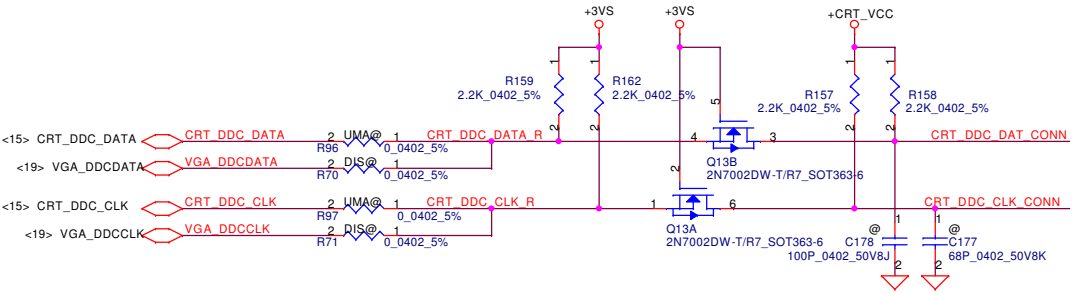
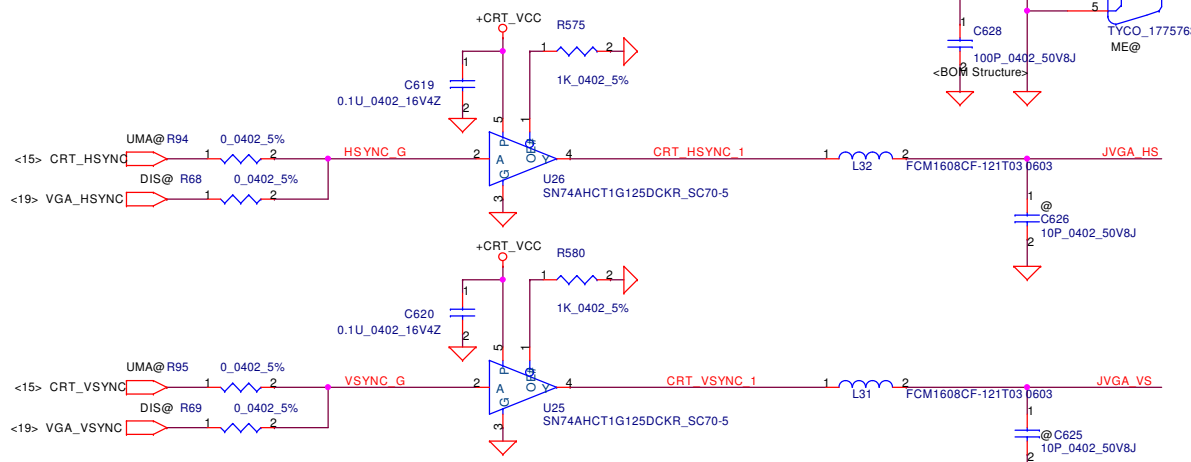
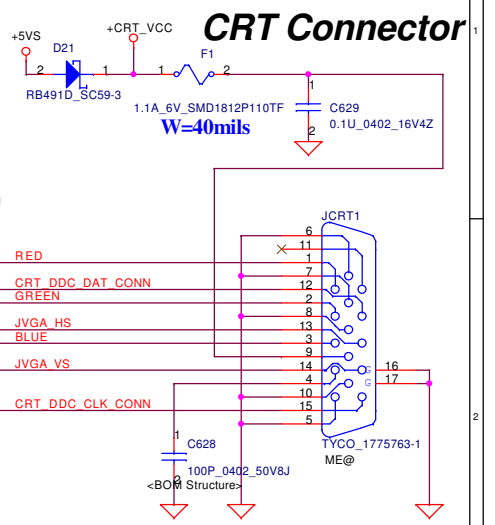
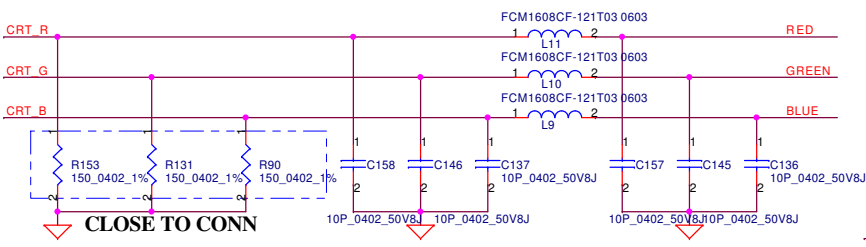
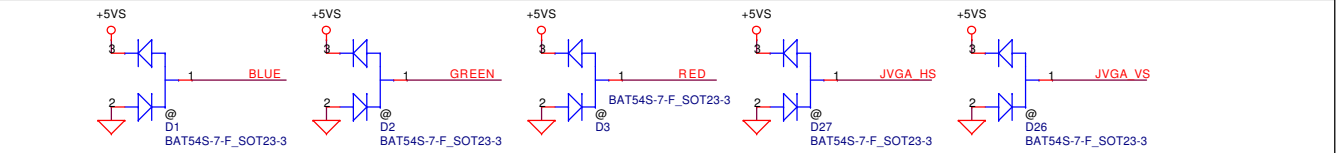
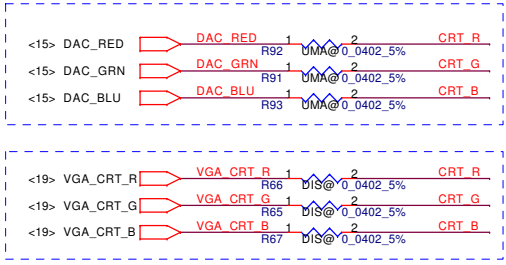
P/N:SA00002D700 (8101T)
P/N:SA00001U900 (CH7318A)

FOR asmedia R428 STUFF
RESERVE THE R668 PULL UP TO 3VS
RESERVE THE R670 PULL DOWN TO GND
CHANGE R483 FROM 499 TO 3.4K OHM

FOR 7318C PIN6 PULL DOWN 1.2Kohm
PIN7 PULL DOWN 7.5Kohm
PIN7 PULL UP 20Kohm

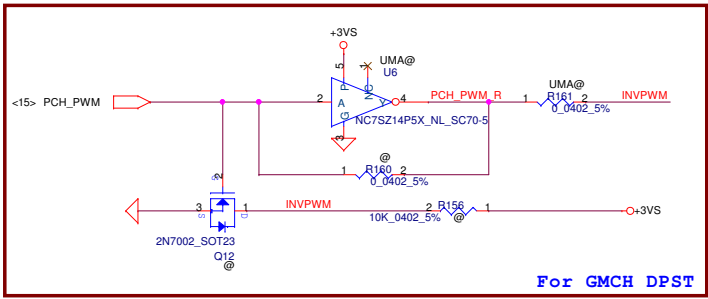
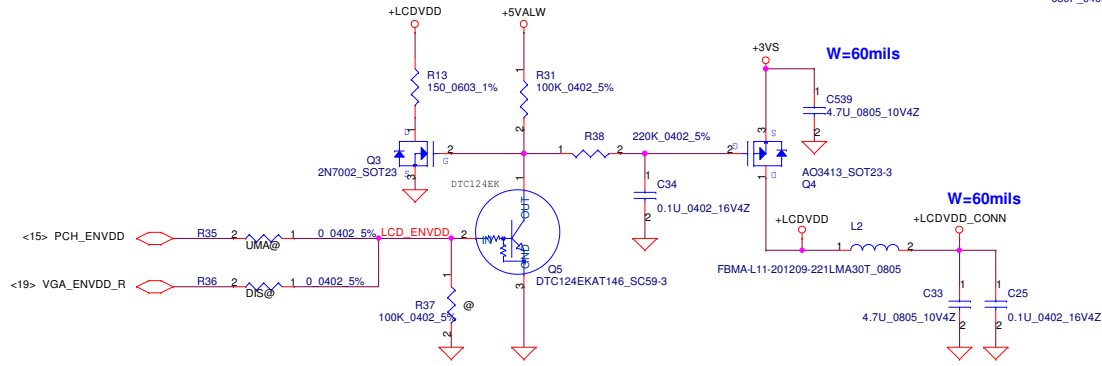


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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Level Shifter_ASM1442
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				Custom	LA-5752P
				Date	Thursday, October 29, 2009
				Sheet	25 of 51
				Rev	0.3

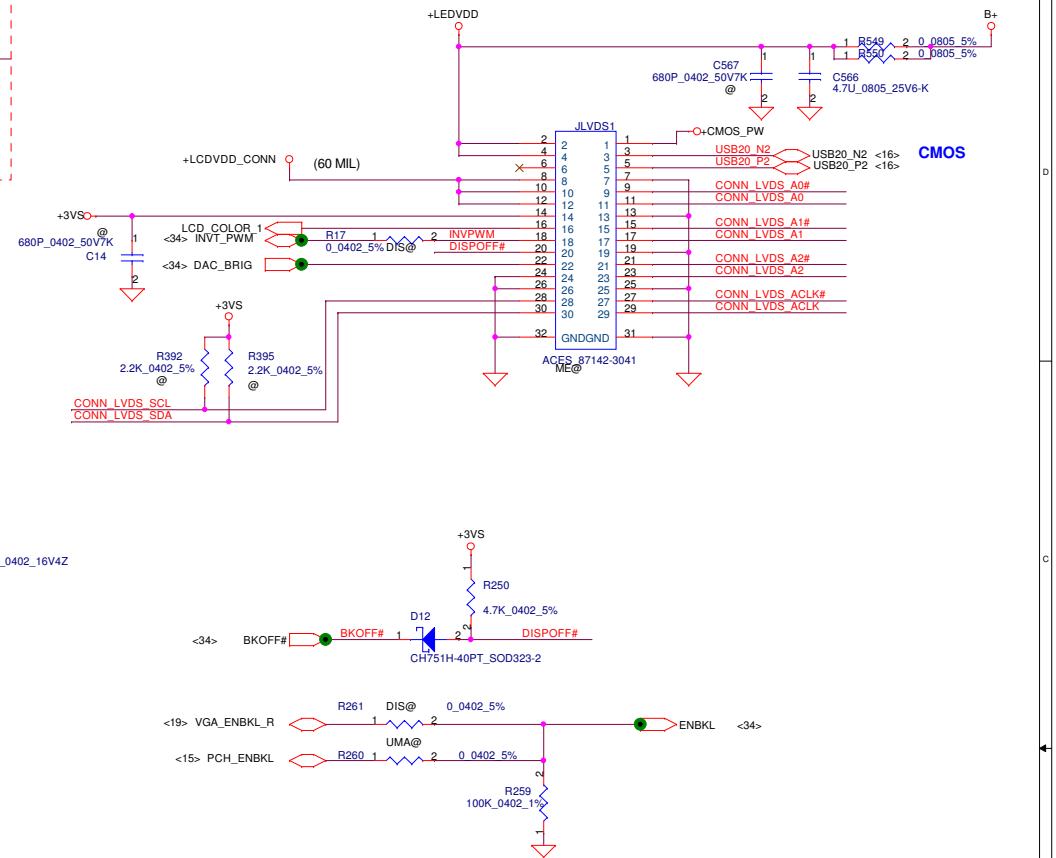
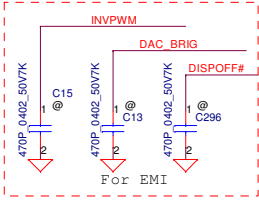


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Size	Document Number	Rev		0.3	
Custom	LA-5752P				
Date:	Thursday, October 29, 2009	Sheet	26	of	51

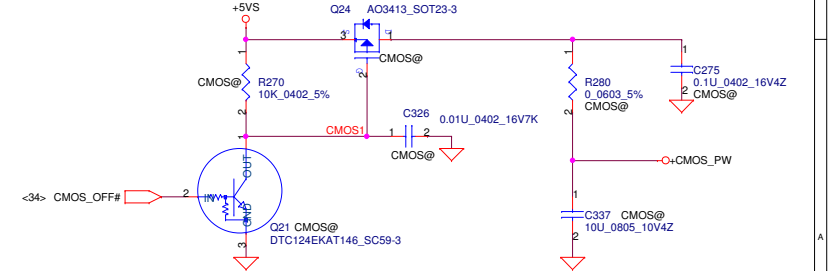
LCD POWER CIRCUIT



<19> VGA_LVDS_SCL	VGA_LVDS_SCL	0.0402_5%	2	DIS@	1	R390	CONN_LVDS_SCL
<19> VGA_LVDS_SDA	VGA_LVDS_SDA	0.0402_5%	2	DIS@	1	R391	CONN_LVDS_SDA
<20> VGA_LVDS_A0	VGA_LVDS_A0	0.0402_5%	2	DIS@	1	R86	CONN_LVDS_A0
<20> VGA_LVDS_A0#	VGA_LVDS_A0#	0.0402_5%	2	DIS@	1	R85	CONN_LVDS_A0#
<20> VGA_LVDS_A1	VGA_LVDS_A1	0.0402_5%	2	DIS@	1	R150	CONN_LVDS_A1
<20> VGA_LVDS_A1#	VGA_LVDS_A1#	0.0402_5%	2	DIS@	1	R128	CONN_LVDS_A1#
<20> VGA_LVDS_A2	VGA_LVDS_A2	0.0402_5%	2	DIS@	1	R126	CONN_LVDS_A2
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<20> VGA_LVDS_ACLK	VGA_LVDS_ACLK	0.0402_5%	2	DIS@	1	R84	CONN_LVDS_ACLK
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<15> EDID_CLK	EDID_CLK	0.0402_5%	2	UMA@	1	R393	CONN_LVDS_SCL
<15> EDID_DATA	EDID_DATA	0.0402_5%	2	UMA@	1	R394	CONN_LVDS_SDA
<15> LVDS_A0	LVDS_A0	0.0402_5%	2	UMA@	1	R383	CONN_LVDS_A0
<15> LVDS_A0#	LVDS_A0#	0.0402_5%	2	UMA@	1	R382	CONN_LVDS_A0#
<15> LVDS_A1	LVDS_A1	0.0402_5%	2	UMA@	1	R389	CONN_LVDS_A1
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<15> LVDS_A2	LVDS_A2	0.0402_5%	2	UMA@	1	R386	CONN_LVDS_A2
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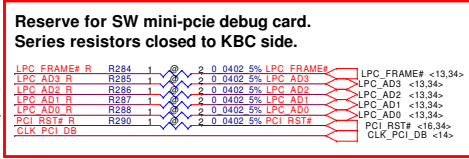
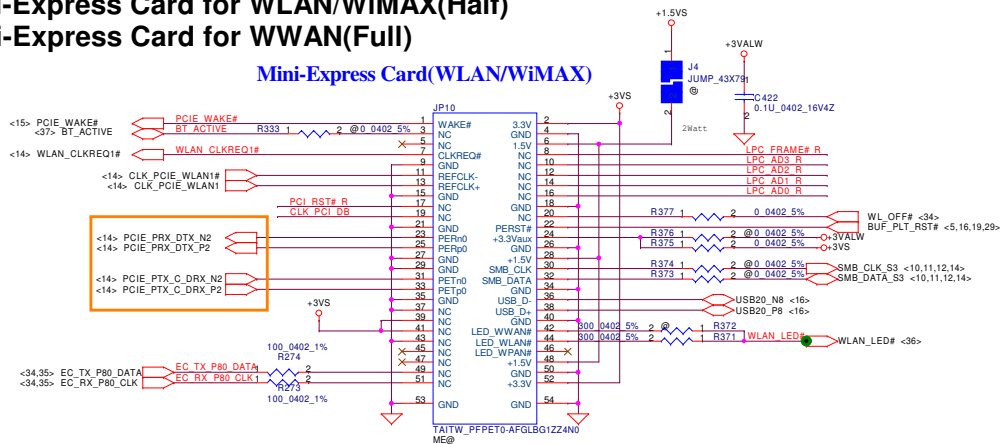
CMOS Camera



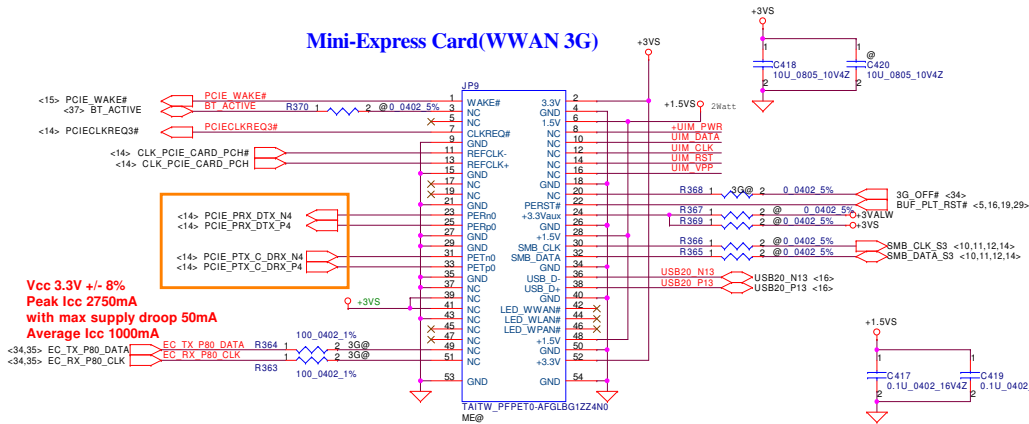
Security Classification	Compal Secret Data			Title	Compal Electronics, Inc.		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	LVDS/CAMERA			
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				B	LA-5752P	0.3	
				Date:	Thursday, October 29, 2009	1	Sheet 27 of 51

Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for WWAN(Full)

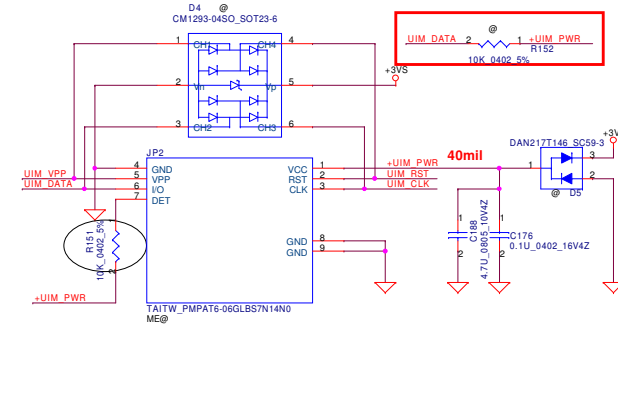
Mini-Express Card(WLAN/WiMAX)



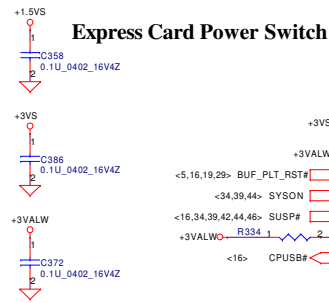
Mini-Express Card(WWAN 3G)



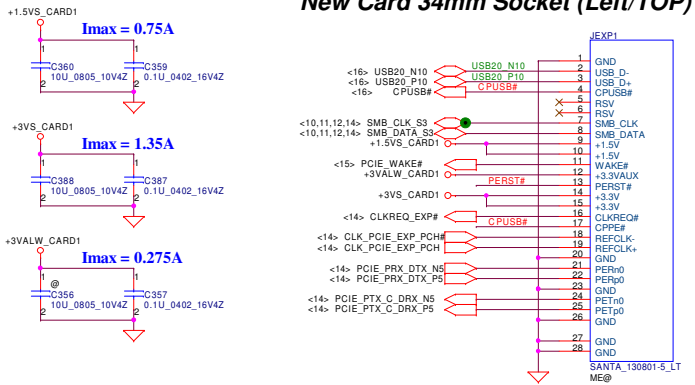
Vcc 3.3V +/- 0%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

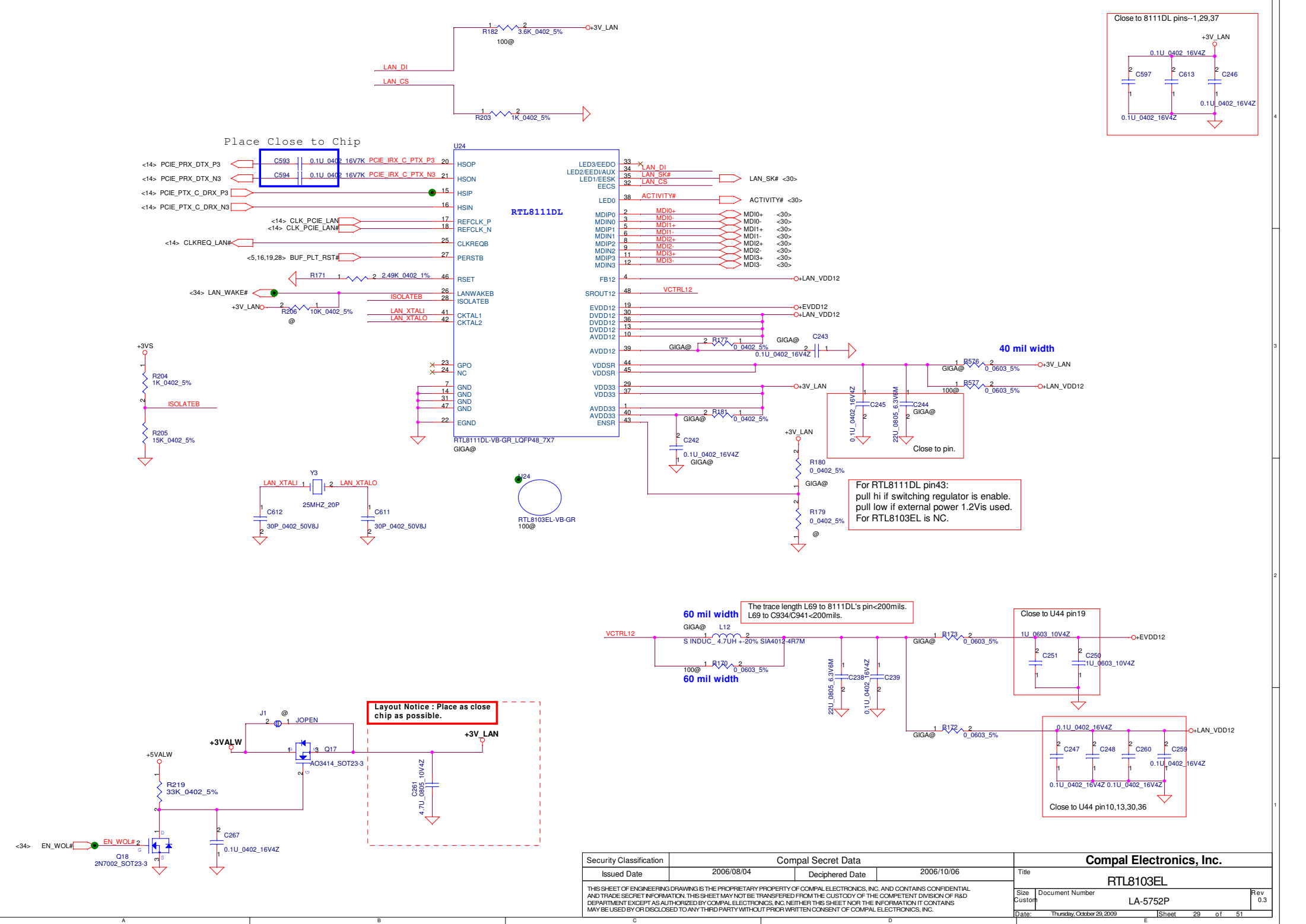


Express Card Power Switch



New Card 34mm Socket (Left/TOP)





Place Close to Chip

RTL8111DL

RTL8103EL-VB-GR 100@

For RTL8111DL pin43:
pull hi if switching regulator is enable.
pull low if external power 1.2Vis used.
For RTL8103EL is NC.

The trace length L69 to 8111DL's pin<200mils.
L69 to C934/C941<200mils.

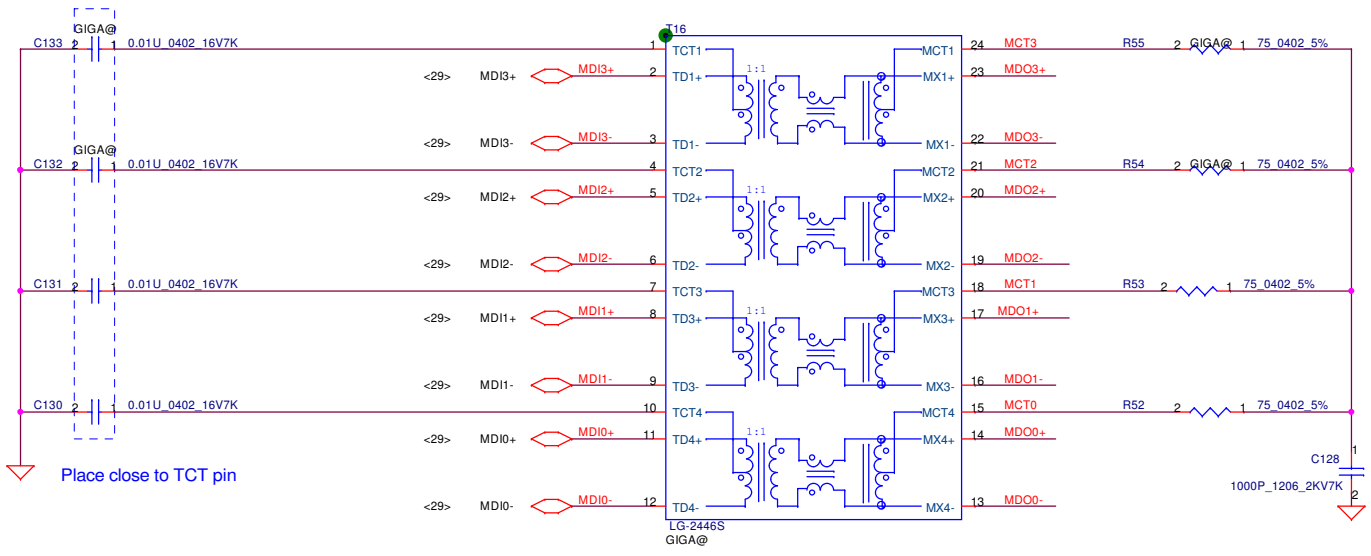
Close to U44 pin19

Close to U44 pin10,13,30,36

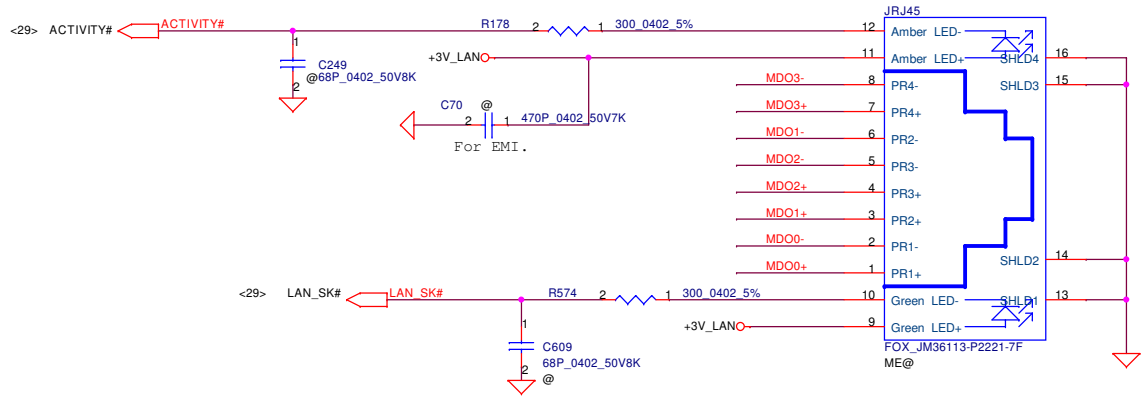
Layout Notice : Place as close
chip as possible.

Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/04	Deciphered Date	2006/10/06	RTL8103EL
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				Document Number LA-5752P
				Rev 0.3
				Date: Thursday, October 29, 2009
				Sheet 29 of 51

Close to T14

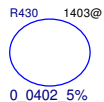


Place close to TCT pin

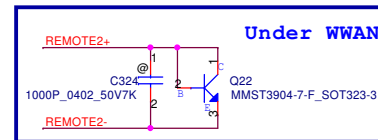
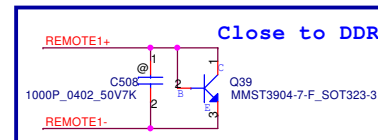
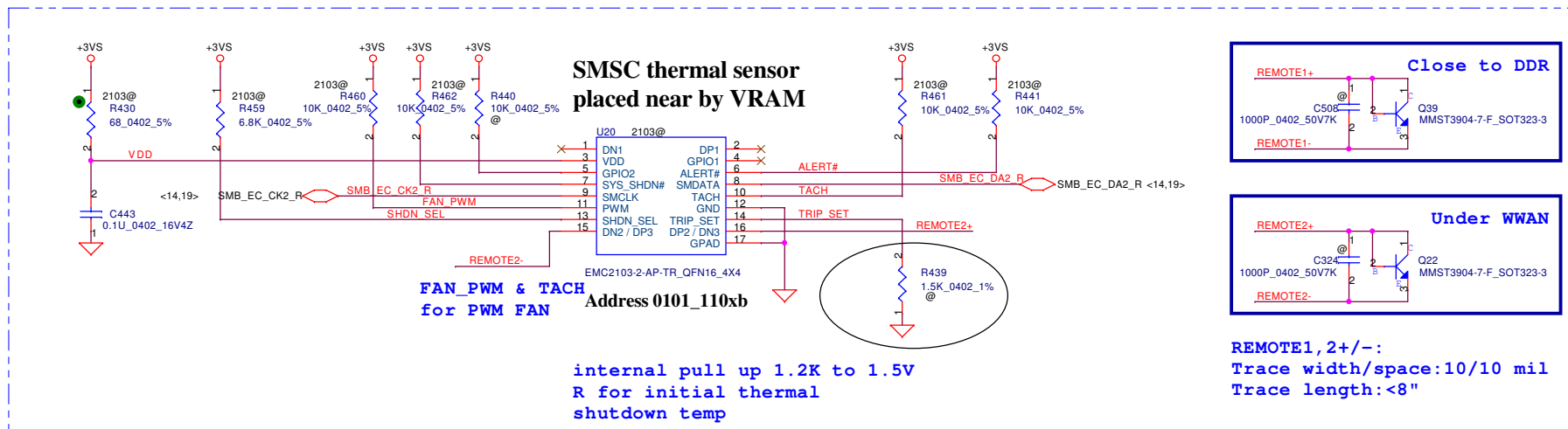


RJ45 Conn.

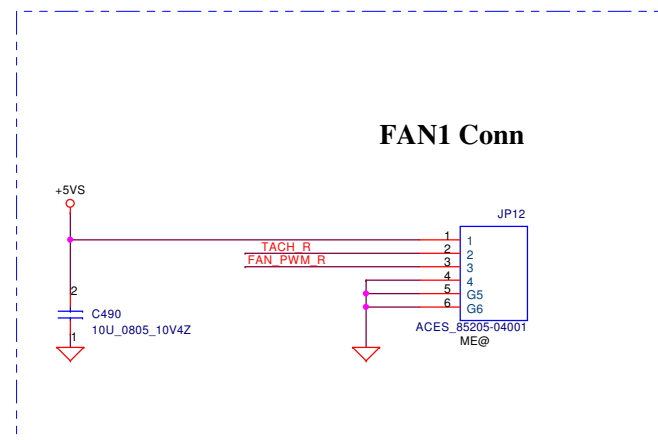
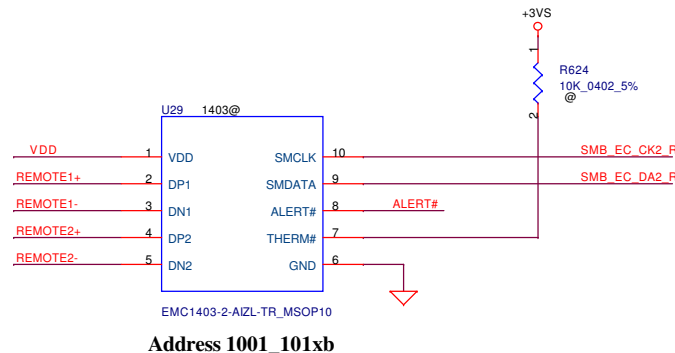
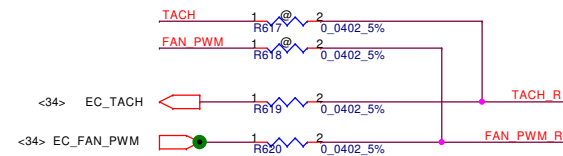
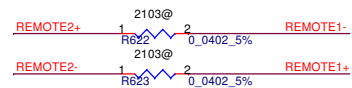
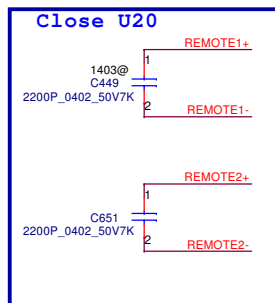
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/03/20	Deciphered Date	2010/03/20	Title	
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Size	Custom	Document Number	LA-5752P	Rev	0.3
Date:	Thursday, October 29, 2009	Sheet	30 of 51		



1403:
@C508/@C324=100p



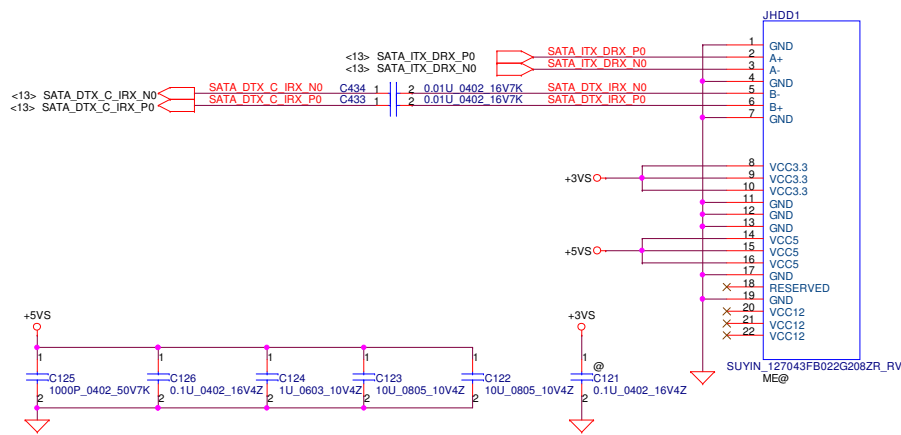
REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"



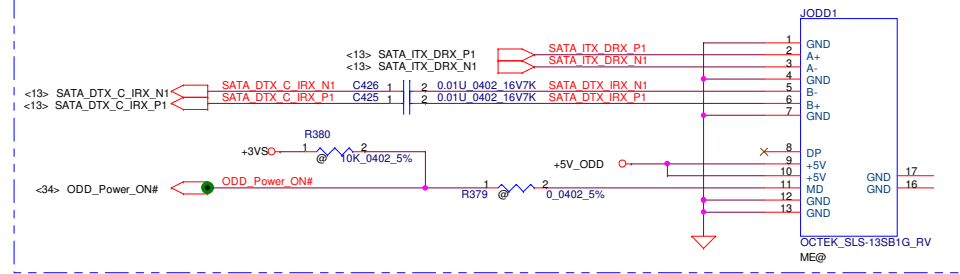
Shutdown Temp	TRIP_SET R439 (1%)
93	953ohm
94	1020ohm
95	1100ohm
96	1150ohm
97	1240ohm
98	1330ohm
99	1400ohm
100	1500ohm
101	1580ohm
102	1690ohm
103	1820ohm
104	1960ohm
105	2050ohm

Security Classification		Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	EMC2103/1403_Thermal sensor/FAN
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Date:	Thursday, October 29, 2009	Sheet	31 of 51	Rev	0.3

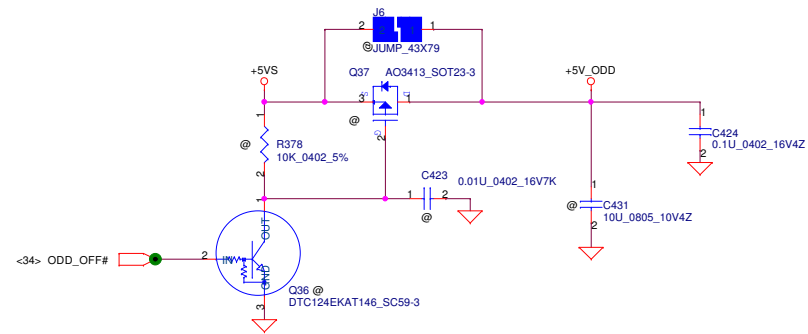
SATA HDD Conn.



SATA ODD Conn.

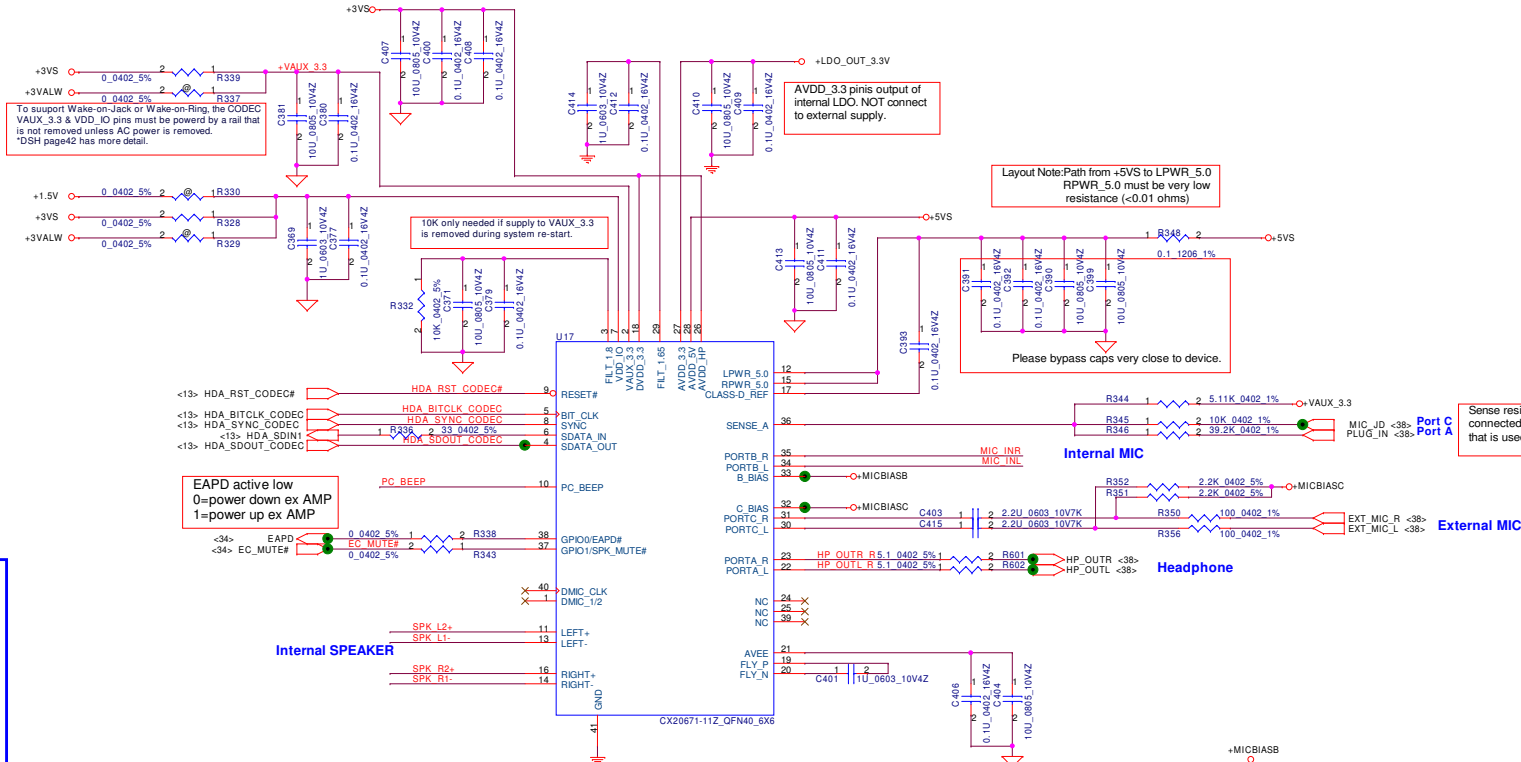
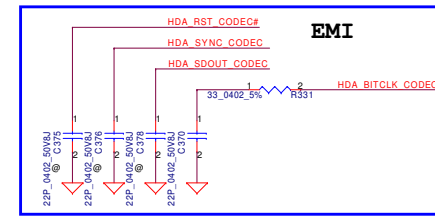


ODD Power Control



Security Classification	Compal Secret Data			Title		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc. HDD/ODD Connector		
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				LA-5752P Date: Thursday, October 29, 2009 Sheet 32 of 51		

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



To support Wake-on-Lack or Wake-on-Ring, the CODEC VAUX_3.3 & VDD_IO pins must be powered by a rail that is not removed unless AC power is removed.
 *DSH page42 has more detail.

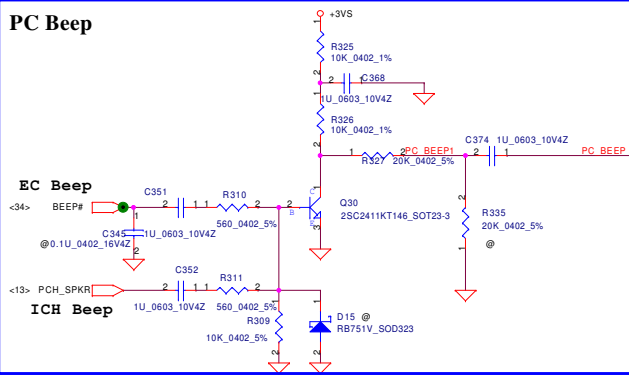
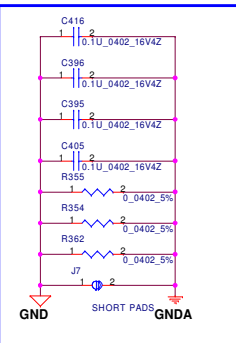
AVDD_3.3 pins output of internal LDO. NOT connect to external supply.

Layout Note: Path from +5VS to LPWR_5.0 RPWR_5.0 must be very low resistance (<0.01 ohms)

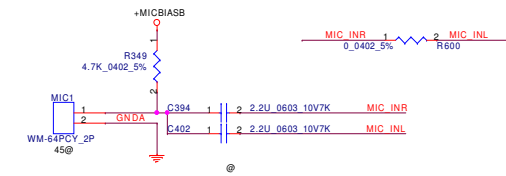
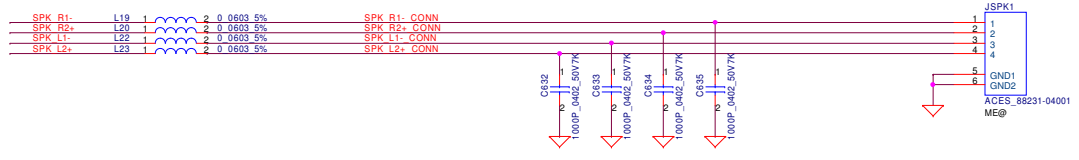
Please bypass caps very close to device.

Sense resistors must be connected same power that is used for VAUX_3.3

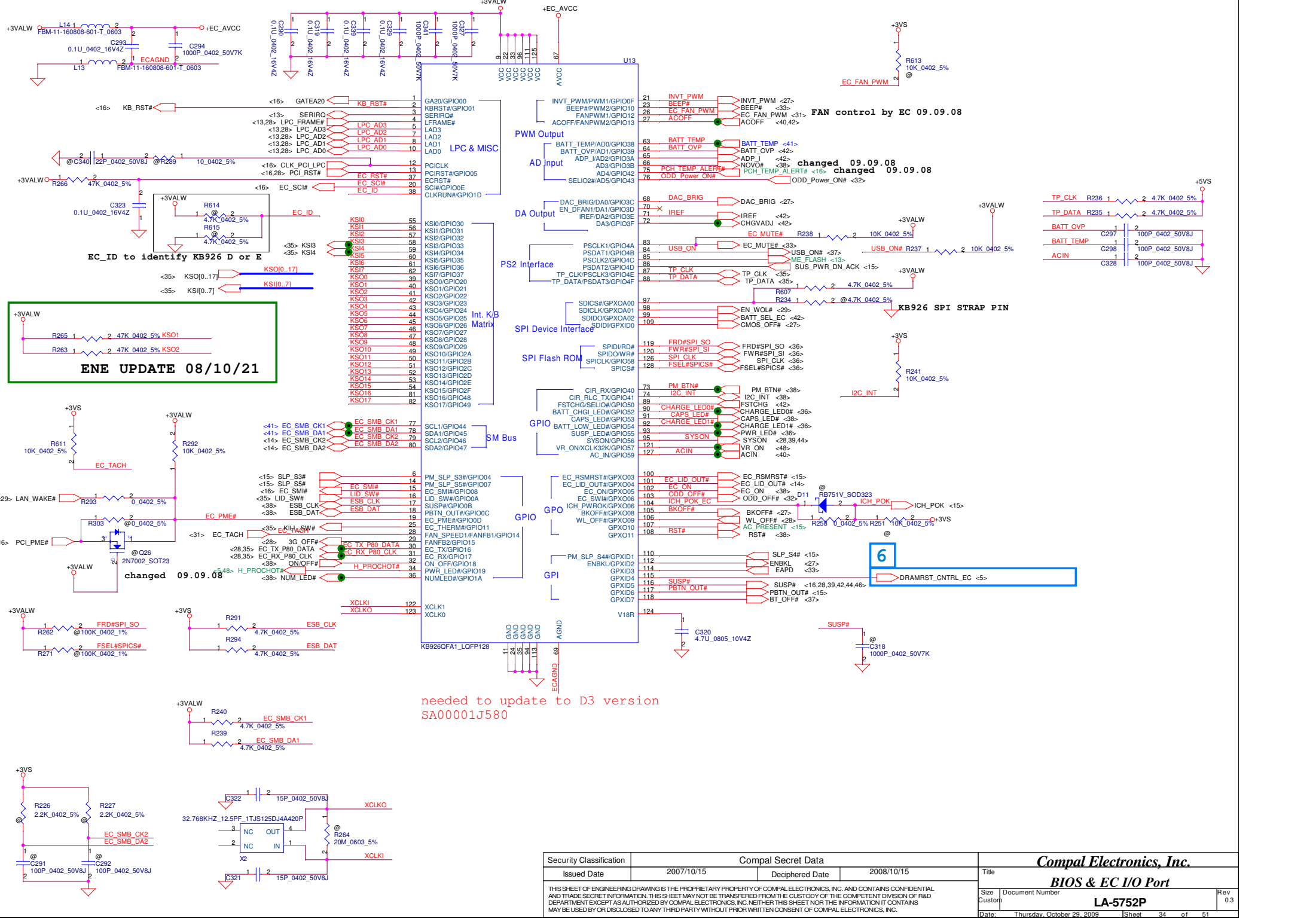
EAPD active low
 0=power down ex AMP
 1=power up ex AMP



wide 20MIL



Security Classification	Compal Secret Data		Title	
Issued Date	2008/03/25	Deciphered Date	2008/04/	CX20671 Codec
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Date: Thursday, October 29, 2009				Sheet 33 of 51



needed to update to D3 version
SA00001J580

Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	BIOS & EC I/O Port
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Size	Document Number	Rev		
Custom	LA-5752P	0.3		
Date:	Thursday, October 29, 2009	Sheet	34	of 51

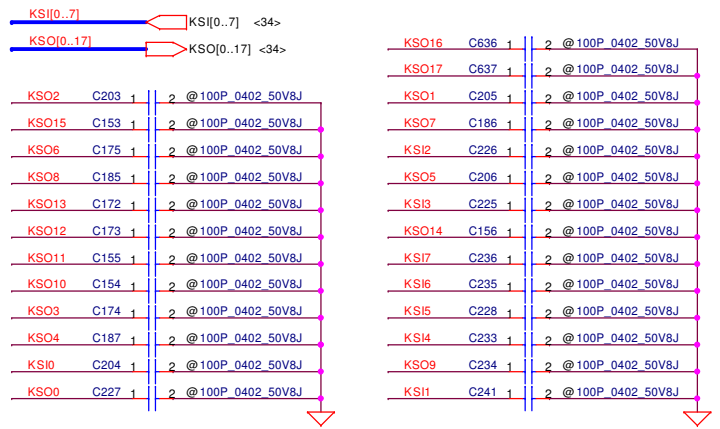
Compal Electronics, Inc.

BIOS & EC I/O Port

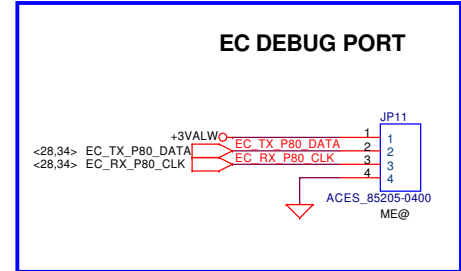
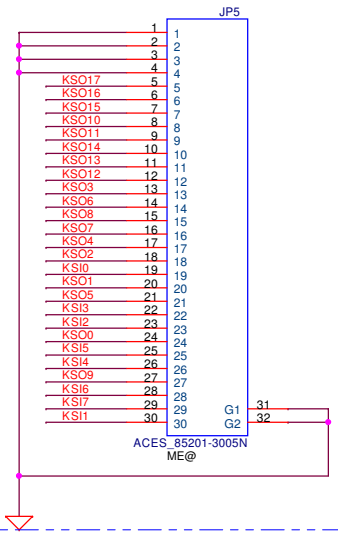
LA-5752P

Size: Document Number: Rev: 0.3
Date: Thursday, October 29, 2009 Sheet: 34 of 51

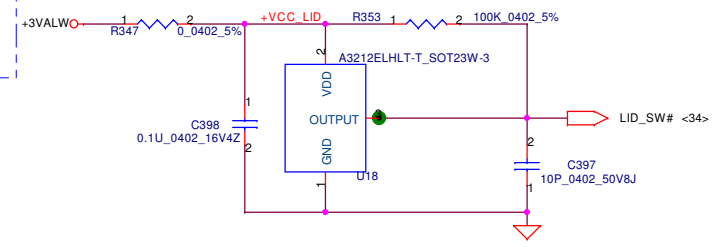
INT_KBD Conn.



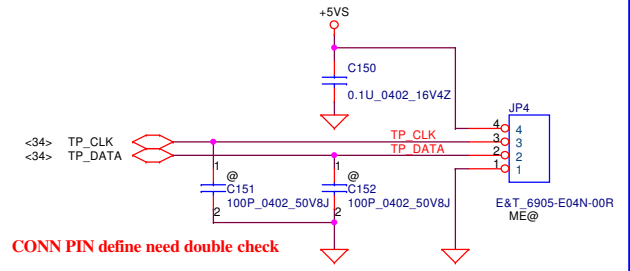
reversal of NIWE1



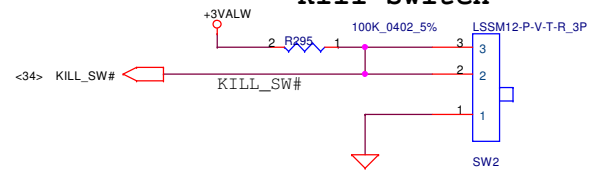
Lid Switch



To TP/B Conn.

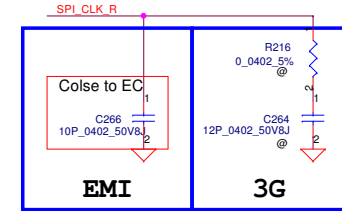
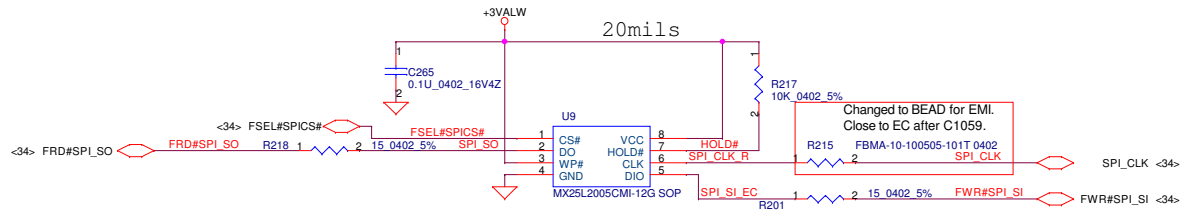


Kill Switch



Kill	
STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

**FOR EC 256KB SPI ROM
(150mil PACKAGE)
P/N : SA00003GK00**

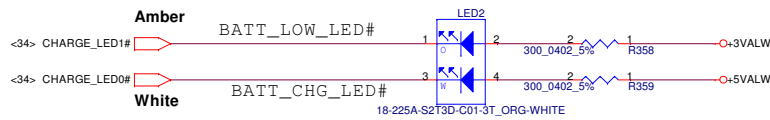


LED

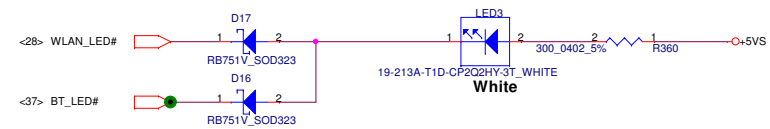
SC500005B00



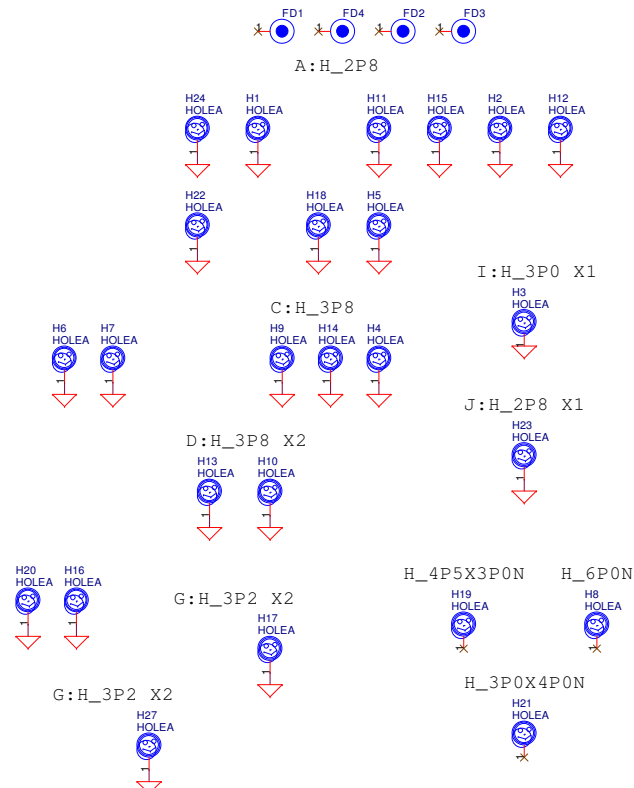
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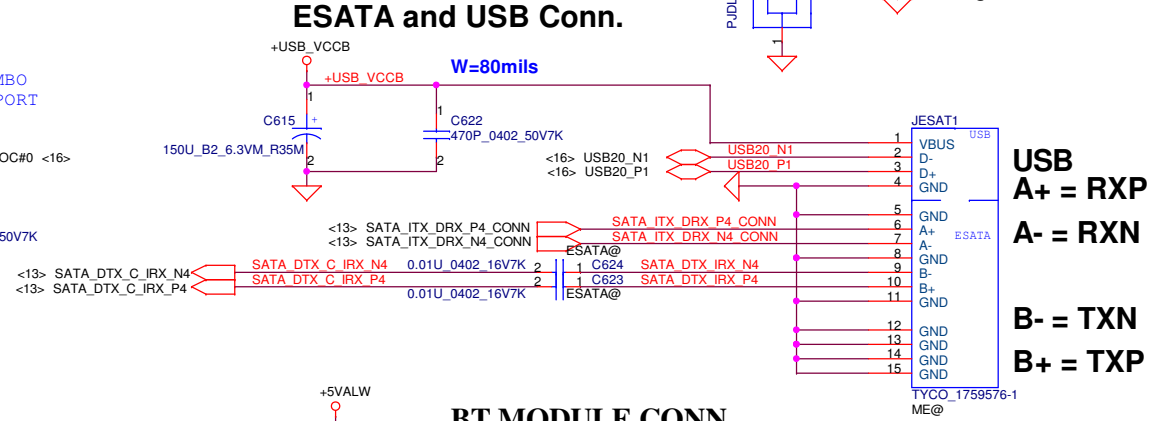
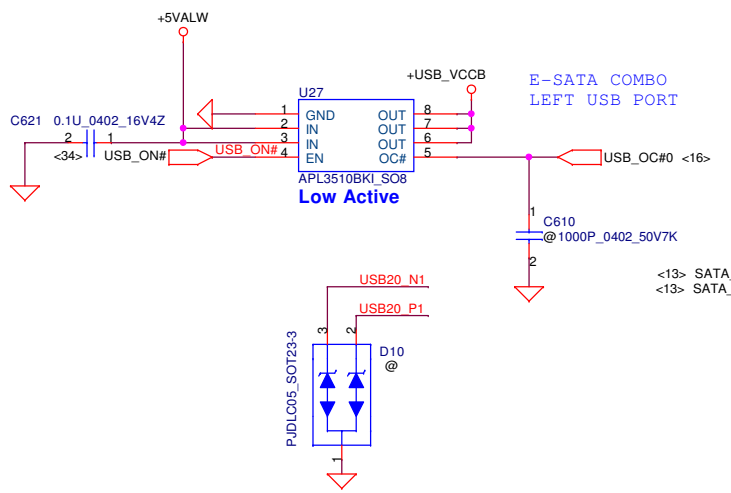
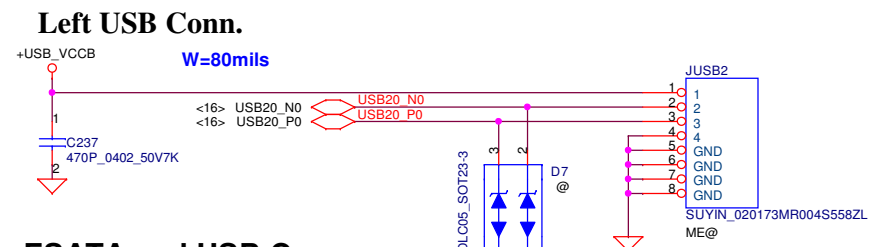
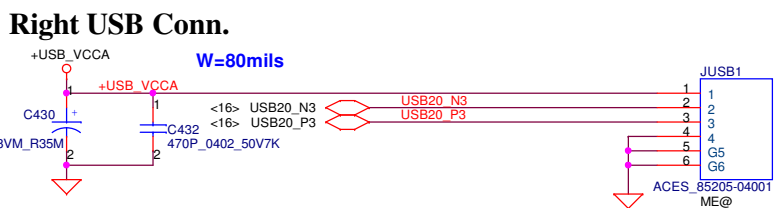
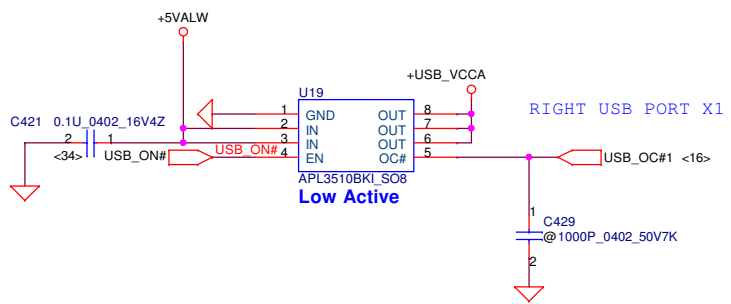
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SC500005B00



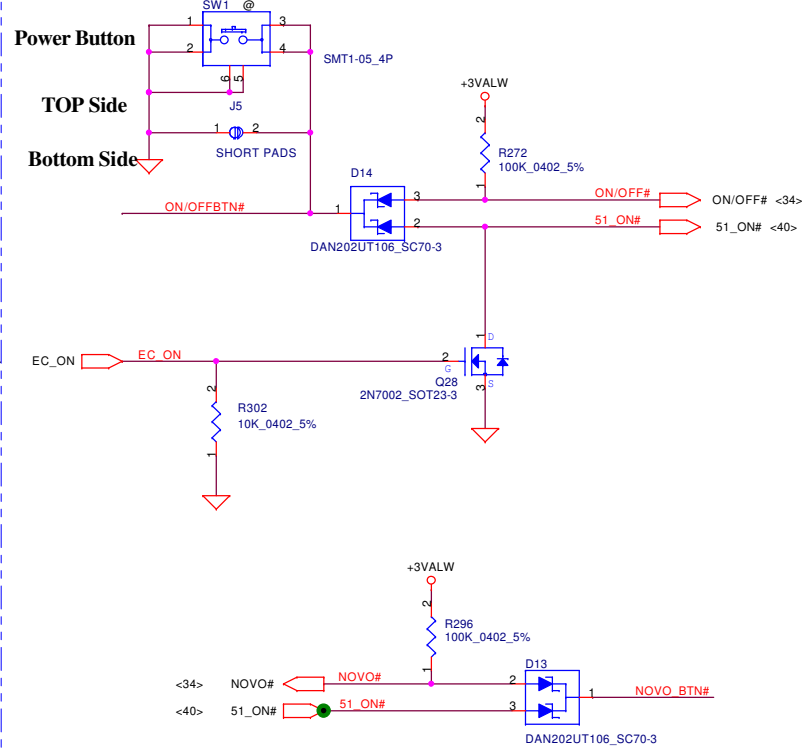
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Issued Date	2007/10/15	Deciphered Date			2008/10/15	
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Size	B		Document Number	LA-5752P	Rev	0.3
Date:	Thursday, October 29, 2009		Sheet	36	of	51



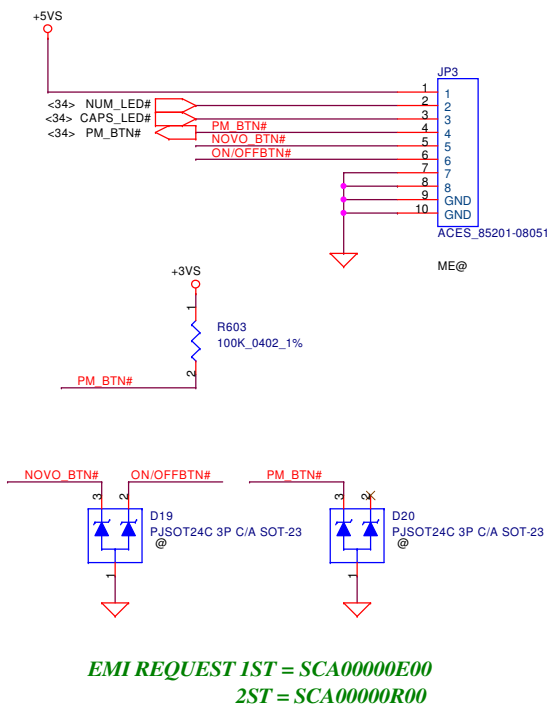
USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				Custom	0.3
				LA-5752P	
Date:		Thursday, October 29, 2009		Sheet 37 of 51	

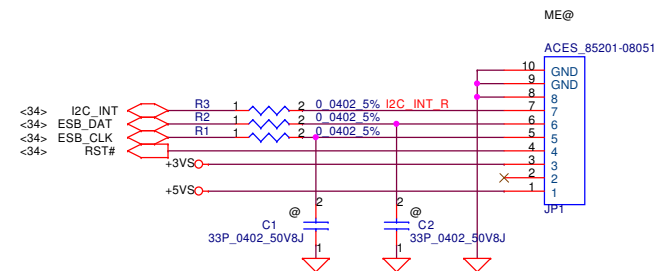
ON/OFF switch



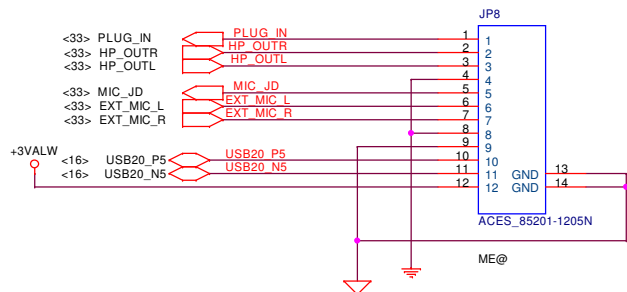
Power Bottom Board Conn. 8pin



Cap Sensor Board Conn. 6pin ENE SB3534

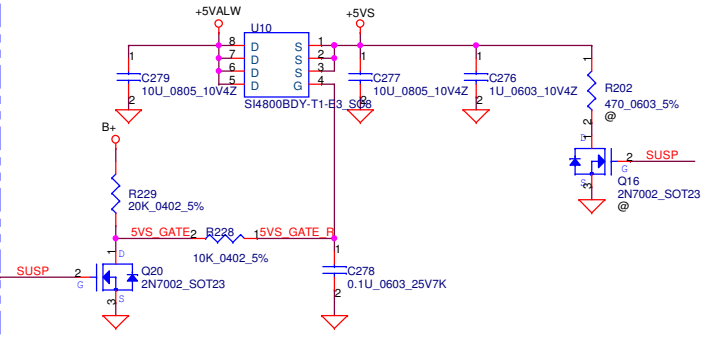


Card Reader/Audio Jack SB CONN

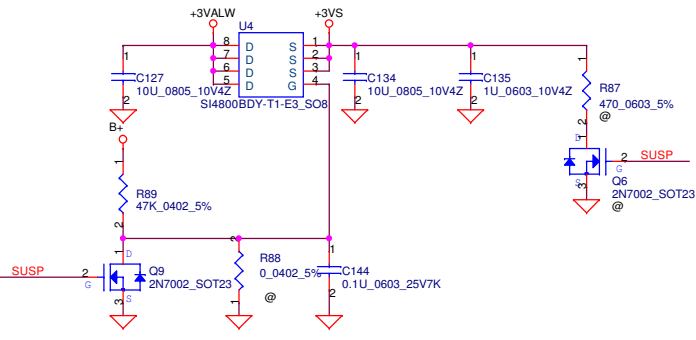


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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title
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Size	Document Number	LA-5752P		Rev
Custom				0.3
Date:	Thursday, October 29, 2009	Sheet	38 of 51	

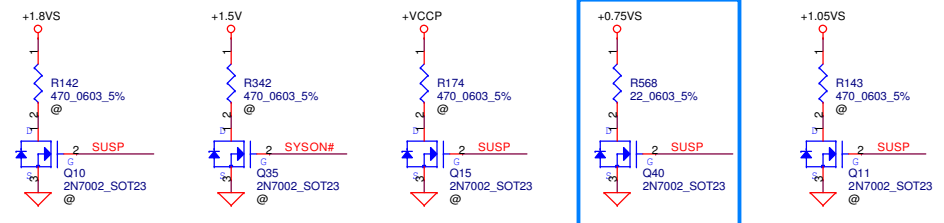
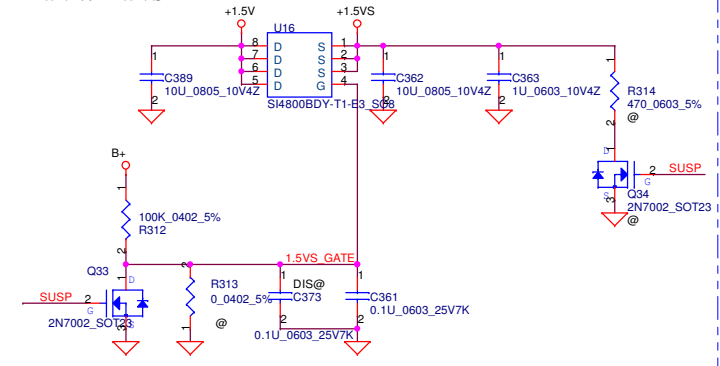
+5VALW TO +5VS



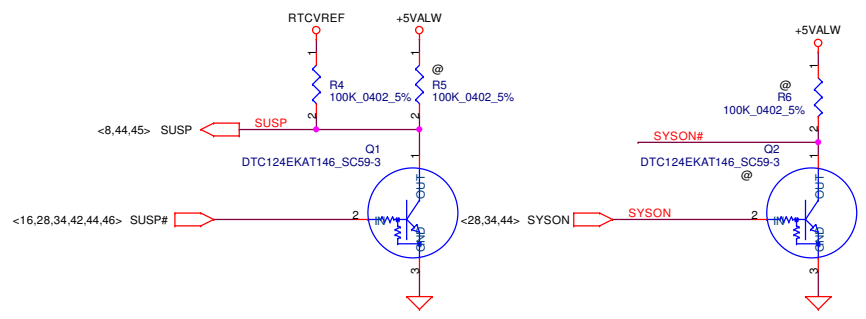
+3VALW TO +3VS



+1.5V to +1.5VS

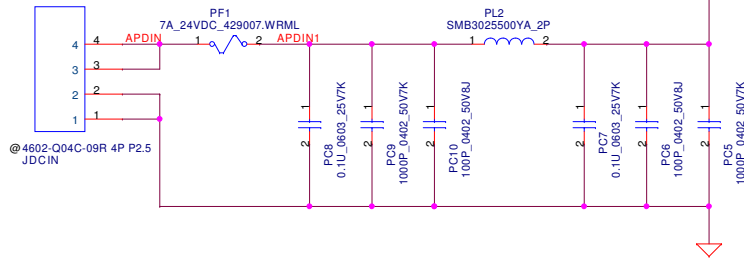


For Intel S3 Power Reduction.



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Issued Date		Deciphered Date		DC Interface	
2006/08/18		2007/8/18		Compal Electronics, Inc.	
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Size	Document Number	Rev		Date	
Custom	LA-5752P	0.3		Thursday, October 29, 2009	
				Sheet	39 of 51

DC030006J00



APDIN1

APDIN

APDIN

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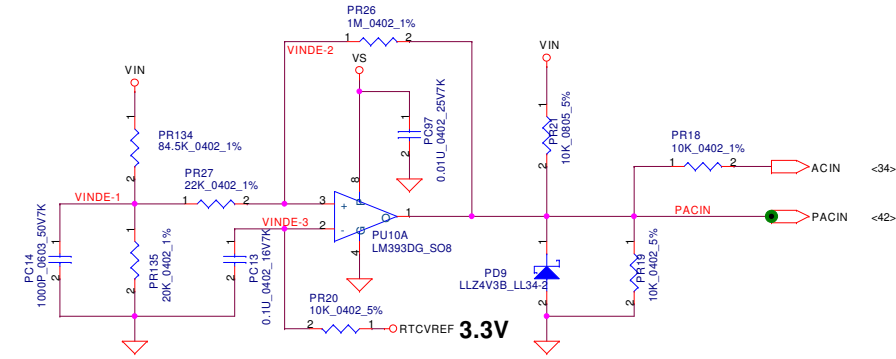
APDIN

APDIN

APDIN

APDIN

Vin Detector			
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



3.3V

VIN

ACIN <34>

PACIN <42>

VS

CHGRTCP

RTCVREF

3.3V

CHGRTCP

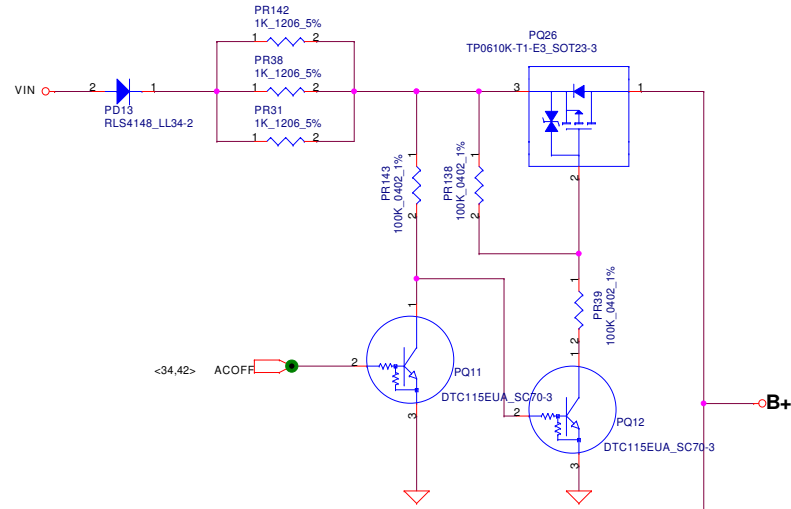
CHGRTCP

CHGRTCP

CHGRTCP

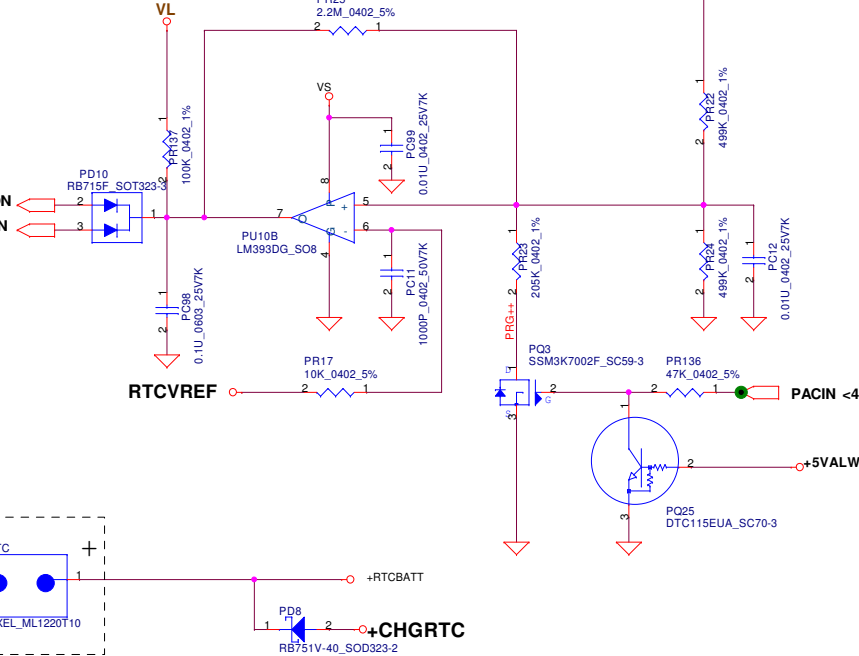
ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V



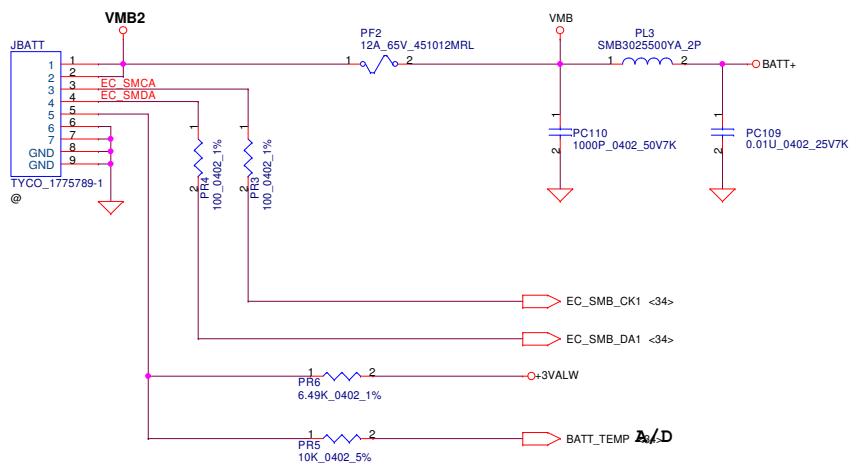
BATT ONLY

Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



RTC Battery

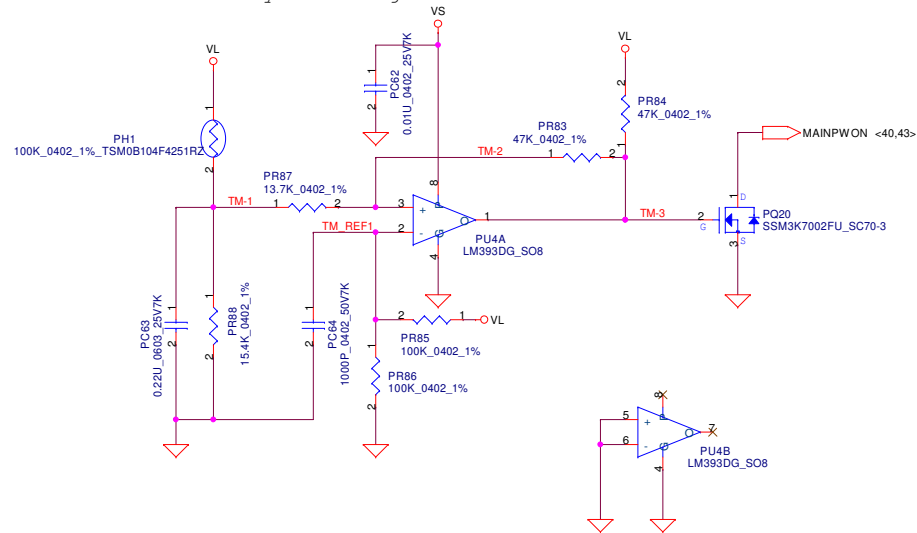
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title
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				Rev
				0.1
Date:	Thursday, October 29, 2009	Sheet	40	of 51



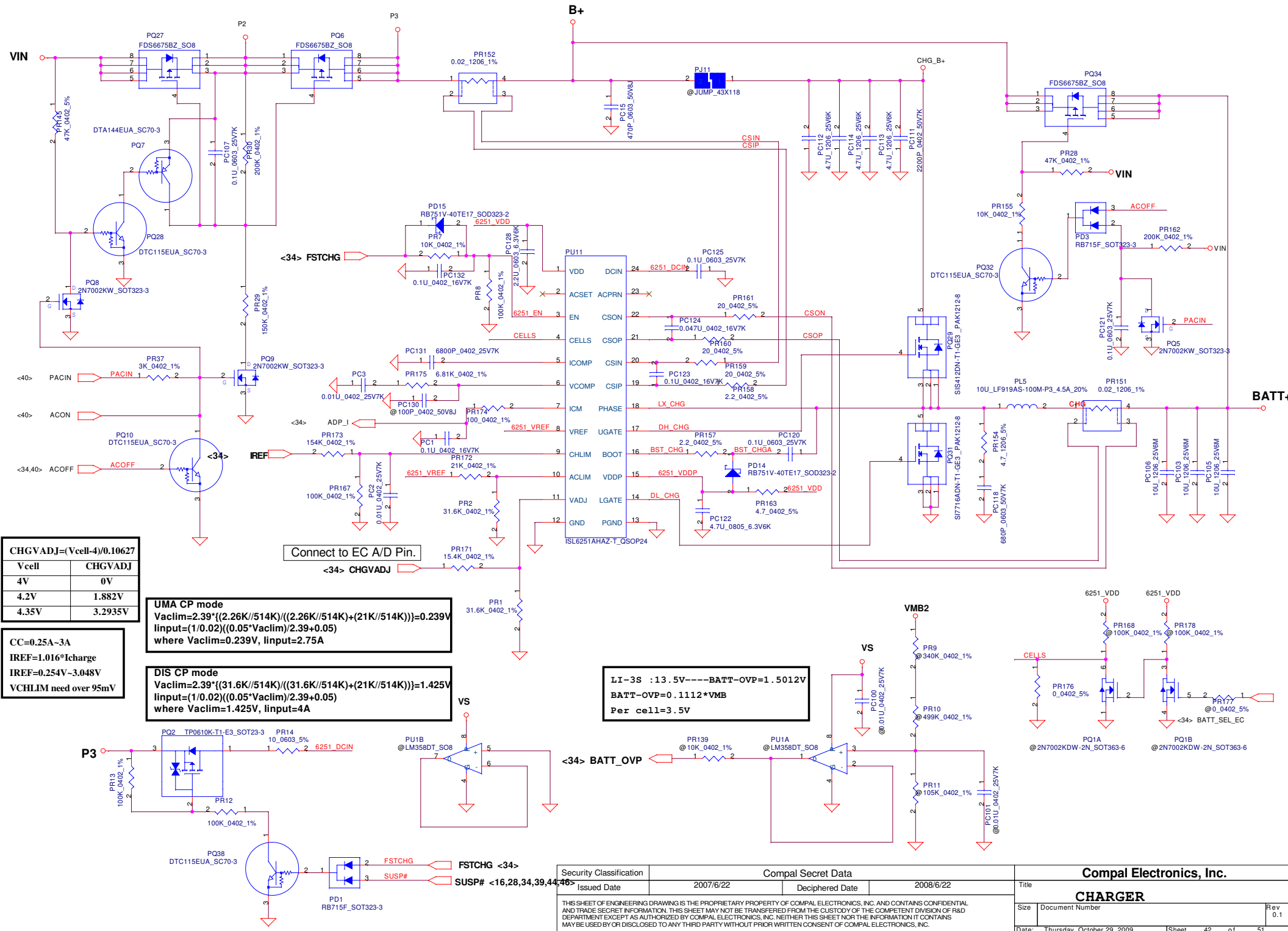
PH1 under CPU bottom side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C



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Size	Document Number			Rev	
Date:	Thursday, October 29, 2009	Sheet	41	of	51
					0.1



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A	
IREF=1.016*Icharge	
IREF=0.254V-3.048V	
VCHLIM need over 95mV	

UMA CP mode
 $V_{aclip} = 2.39 * ((2.26K/514K) / ((2.26K/514K) + (21K/514K))) = 0.239V$
 $I_{input} = (1/0.02) * ((0.05 * V_{aclip}) / (2.39 + 0.05))$
 where $V_{aclip} = 0.239V$, $I_{input} = 2.75A$

DIS CP mode
 $V_{aclip} = 2.39 * ((31.6K/514K) / ((31.6K/514K) + (21K/514K))) = 1.425V$
 $I_{input} = (1/0.02) * ((0.05 * V_{aclip}) / (2.39 + 0.05))$
 where $V_{aclip} = 1.425V$, $I_{input} = 4A$

LI-3S : 13.5V --- BATT-OVP = 1.5012V
BATT-OVP = 0.1112 * VMB
Per cell = 3.5V

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

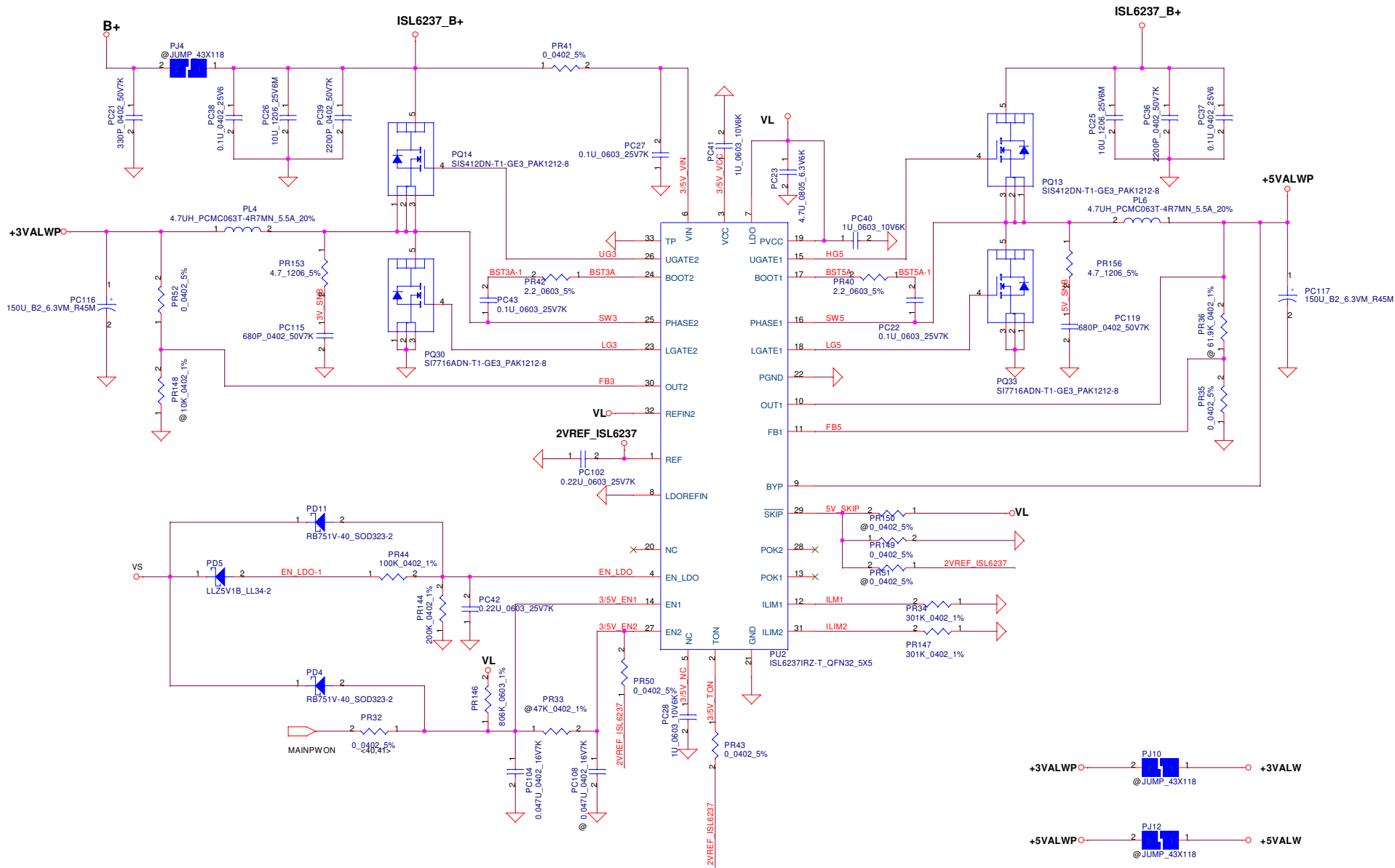
CC=0.25A-3A	
IREF=1.016*Icharge	
IREF=0.254V-3.048V	
VCHLIM need over 95mV	

UMA CP mode
 $V_{aclip} = 2.39 * ((2.26K/514K) / ((2.26K/514K) + (21K/514K))) = 0.239V$
 $I_{input} = (1/0.02) * ((0.05 * V_{aclip}) / (2.39 + 0.05))$
 where $V_{aclip} = 0.239V$, $I_{input} = 2.75A$

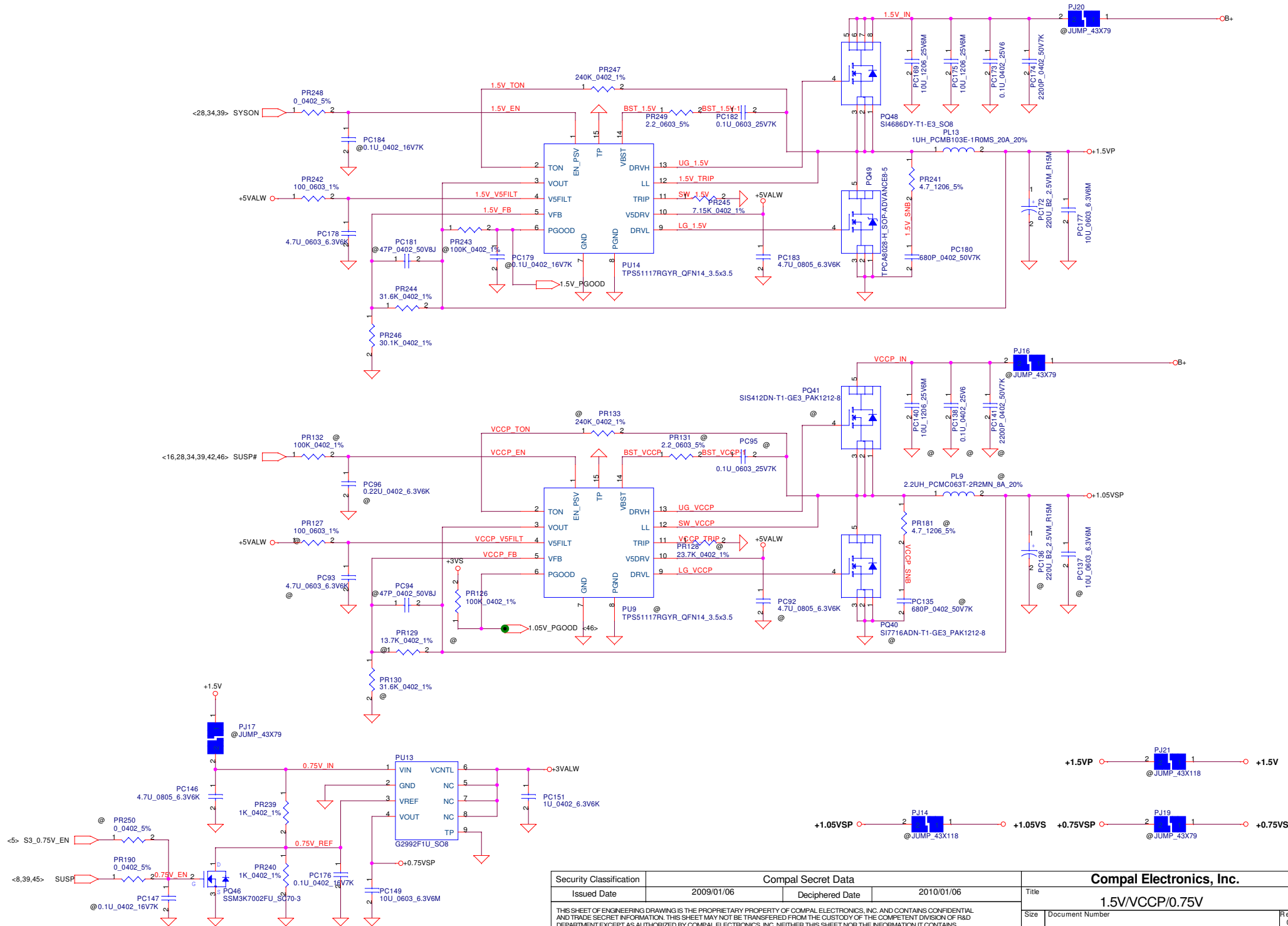
DIS CP mode
 $V_{aclip} = 2.39 * ((31.6K/514K) / ((31.6K/514K) + (21K/514K))) = 1.425V$
 $I_{input} = (1/0.02) * ((0.05 * V_{aclip}) / (2.39 + 0.05))$
 where $V_{aclip} = 1.425V$, $I_{input} = 4A$

LI-3S : 13.5V --- BATT-OVP = 1.5012V
BATT-OVP = 0.1112 * VMB
Per cell = 3.5V

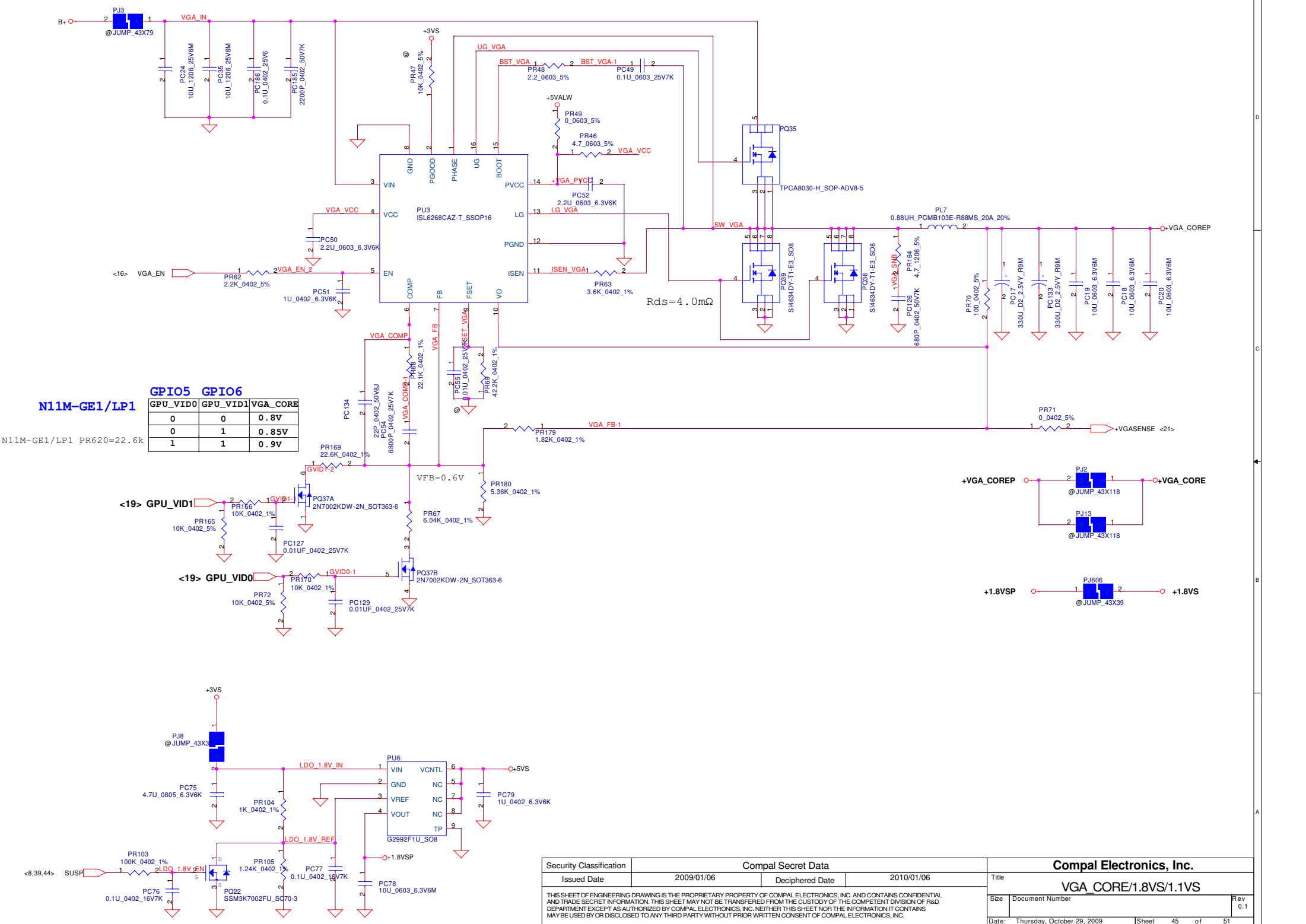
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Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title
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				Document Number
				Rev
				0.1
Date: Thursday, October 29, 2009		Sheet 42 of 51		



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Date: Thursday, October 29, 2009				Sheet 43 of 51
Rev 0.1				



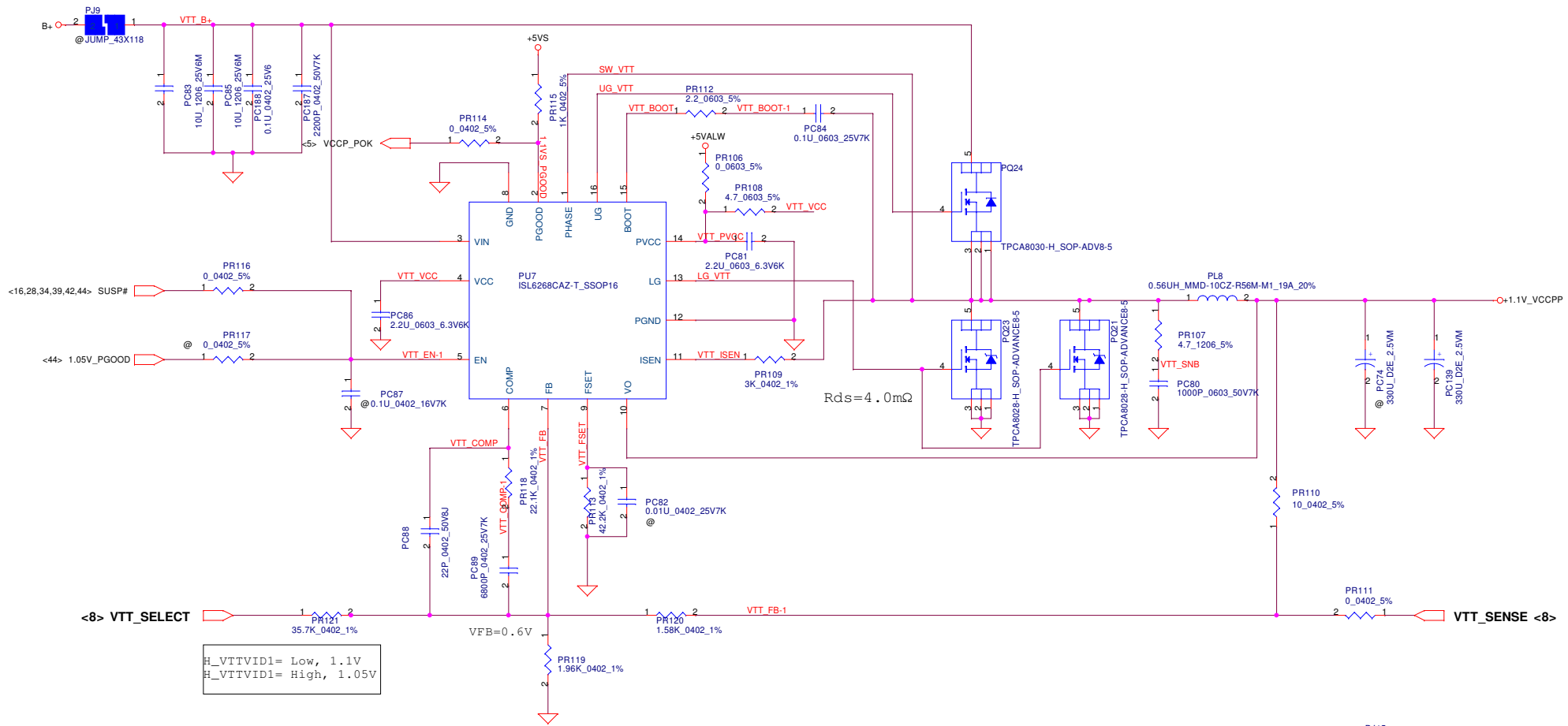
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Date:	Thursday, October 29, 2009	Sheet	44	of	51



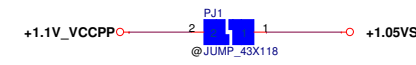
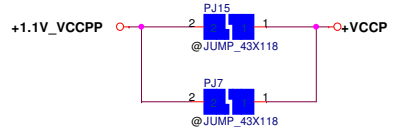
N11M-GE1/LP1 PR620=22.6k

GPIO5		GPIO6	
GPU_VID0	GPU_VID1	VGA_CORE	
0	0	0.8V	
0	1	0.85V	
1	1	0.9V	

Security Classification	Compal Secret Data		Title VGA_CORE/1.8VS/1.1VS
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Date:	Thursday, October 29, 2009	Sheet	45 of 51



H_VTTVID1= Low, 1.1V
H_VTTVID1= High, 1.05V



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				Document Number
				Rev 0.1
				Date: Thursday, October 29, 2009
				Sheet 46 of 51

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
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15					
16					
17				20081022	

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				Size	Document Number
		Custom	<Doc>	0.1	
Date:		Thursday, October 29, 2009		Sheet	49 of 51

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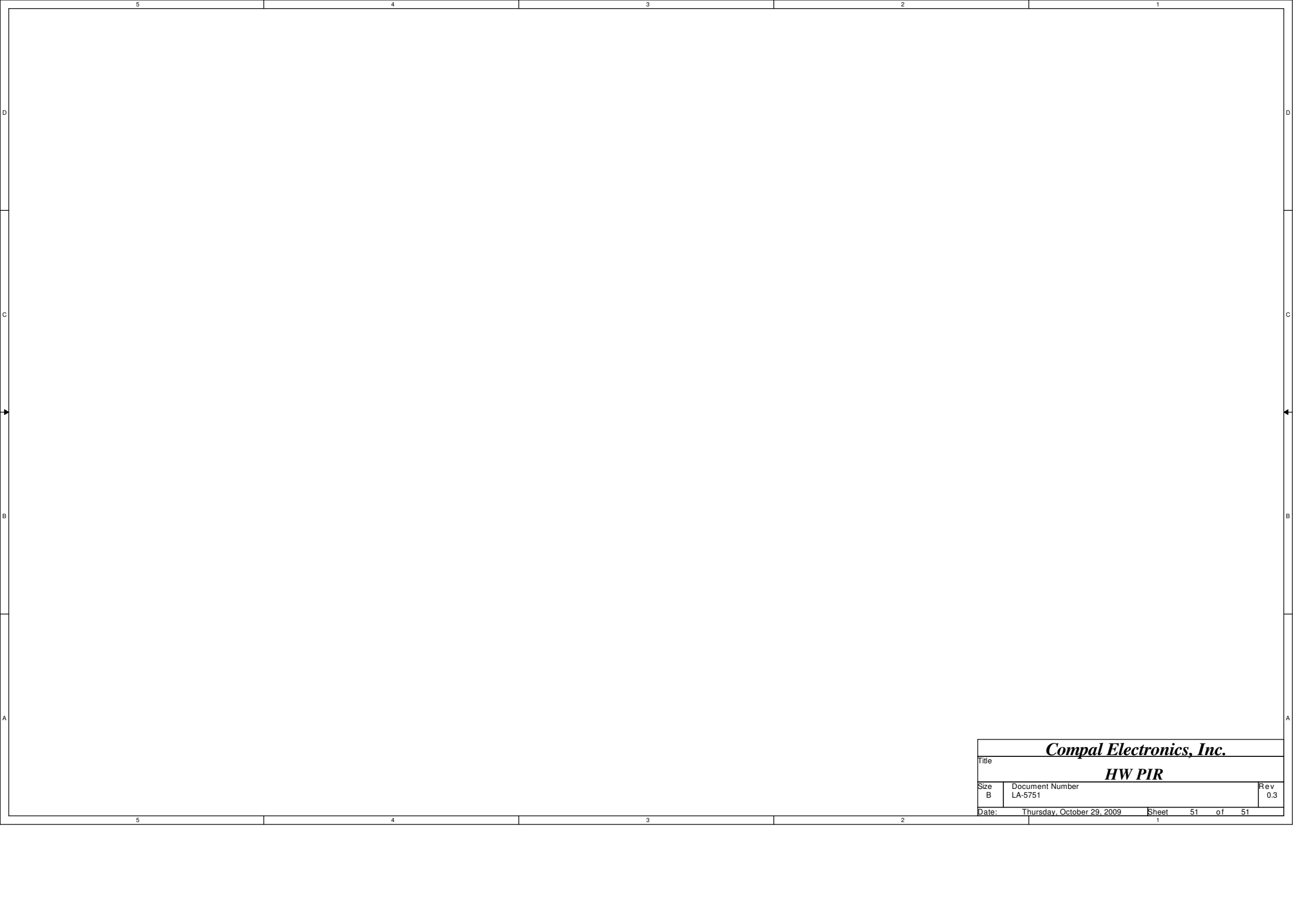
B

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A

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<i>Compal Electronics, Inc.</i>		
Title		
<i>HW PIR</i>		
Size	Document Number	Rev
B	LA-5752P	0.3
Date:	Thursday, October 29, 2009	Sheet 50 of 51



<i>Compal Electronics, Inc.</i>			
Title			
<i>HW PIR</i>			
Size	Document Number	Rev	
B	LA-5751	0.3	
Date:	Thursday, October 29, 2009	Sheet	51 of 51